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PERFORMANCE EVALUATION OF VISION ALGORITHMS ON FPGA

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By

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This thesis is submitted to the Department of Electronic &
Telecommunication Engineering
of the University of Moratuwa
in partial fulfillment of the requirements for
the degree of Master of Science in Full Time Research.

University of Moratuwa, Sri Lanka

July, 2010

DECLARATION

I certify that this thesis does not incorporate without acknowledgement any material previously submitted for a degree or diploma in any university. Furthermore, this does not contain any material previously published or written or orally communicated by another person except where due reference is made in the text or in the figure captions or in the table captions.

Mahendr G. Samarawickrama

To the best of our knowledge the above particulars are true and accurate.

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Abstract

The modern FPGAs enable system designers to develop high-performance computing (HPC) applications with large amount of parallelism. Real-time image processing is such a requirement that demands much more processing power than a conventional processor can deliver. In this research, we implemented software and hardware based architectures on FPGA to achieve real-time image processing. Furthermore, we benchmark and compare our implemented architectures with existing architectures. The operational structures of those systems consist of on-chip processors or custom vision coprocessors implemented in a parallel manner with efficient memory and bus architectures. The performance properties such as the accuracy, throughput and efficiency are measured and presented.

According to results, FPGA implementations are faster than the DSP and GPP implementations for algorithms which can exploit a large amount of parallelism. Our image pre-processing architecture is nearly two times faster than the optimized software implementation on an Intel Core 2 Duo GPP. However, because of the higher clock frequency of DSPs/GPPs, the processing speed for sequential computations on on-chip processors in FPGAs is slower than on DSPs/GPPs. These on-chip processors are well suited for multi-processor systems for software level parallelism. Our quad-Microblaze architecture achieved 75-80% performance improvement compared to its single Microblaze counterpart. Moreover, the quad-Microblaze design is faster than the single-powerPC implementation on FPFA. Therefore, multi-processor architecture with customised coprocessors are effective for implementing custom parallel architecture to achieve real time image processing.

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To my parents, family and teachers for giving me constant support and motivation.

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Acknowledgment

I wish to thank my supervisors Dr. Ajith Pasqual and Dr. Ranga Rodrigo for their support and encouragement during this research. Their insight, guidance, feedback and especially the constructive criticisms contributed enormously to the production of this thesis.

I am grateful to Dr. E.C. Kulasekere, the coordinator of this research and Dr. Chathura De Silva, the chairman of the progress review committies and Prof. (Mrs.) I.J. Dayawansa, the postgraduate research advisor for their feedback, kind advice and invaluable suggestions given.

I am deeply indebted to other academics and administrators who have provided helpful advice and knowledge during this research.

I also wish to extend my gratitude to Zone24×7 (Pvt) Ltd. for providing laboratory facilities.

I acknowledge the financial support given by the *University of Moratuwa Senate Research Committee grant SRC-297*, to enable me conduct the masters program at University of Moratuwa.

Finally, I am thankful to my parents, family and friends for their care, commitment and support they extended to me during this research program.

MAHENDRA G. SAMARAWICKRAMA
July 2010

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Abbreviations

Following abbreviations or acronyms have been used in this thesis.

Abbreviations/acronyms	Meaning
ADDR	Address: Memory location for read/write data
BRAM	Block RAM
CLK	Clock
CMP	Chip Multiprocessor
DDR	Double Data Rate
DIN	Data Input: Data written into memory
DOUT	Data Output: Synchronous output of the memory
DSP	Digital Signal Processor
EDK	Embedded Development Kit
EN	Enable: Enables access to memory
EEPROM	Electrically Erasable Programmable ROM
FPGA	Field-Programmable Gate Array
GPP	General Purpose Processor
HDL	Hardware Description Language
HLL	High-Level Language
LMB	Local Memory Bus
LUT	Lookup Table
ROM	Read-Only Memory
PIF	Performance Improve Factor
PLB	Processor Local Bus
SoC	System on Chip
WE	Write Enable: Allows data transfer into memory
XCL	Xilinx Cache Link
XPS	Xilinx Platform Studio

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Nomenclature

Following symbols or notations have been used in this thesis.

Notation	Meaning
T_{nbhd}	Time to read neighborhood pixels around the first pixel of the image
N_{mask}	Kernel dimension
f_{clk}	Clock frequency
T_{img}	Total time needs to process all the pixels of the image
M_{img}	Number of pixels per image
T_{SM}	Time to execute in single-microblaze architecture
T_{QM}	Time to execute in quad-processor-microblaze architecture

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