MULTI-RESOLUTION ANALYSIS BASED ANN ARCHITECTURE FOR FAULT DETECTION IN DC MICROGRIDS

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Degree of Master of Philosophy by Research

Department of Electrical Engineering

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DECLARATION

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ABSTRACT

DC microgrids present an effective means for integration of renewable energy sources to the utility network while offering clear benefits such as higher efficiency, better compatibility with DC sources and loads and simpler control, compared to its AC counterpart. However, protection challenges associated with DC networks, such as lack of frequency and phasor information, lack of standards, guidelines and practical experience are of particular concern.

Lack of effective solutions for protection of DC networks presents a major barrier for the widespread integration of DC microgrids to the utility network. There are several conventional DC network protection techniques employed in wide range of DC network applications in the fields of telecommunication, data centers and shipboard networks. However, straightforward application of these conventional techniques for protection of DC microgrids is impracticable due to intermittent nature of DGs connected to the network, operation in both grid-connected and islanding mode and high sensitivity to fault impedance.

Hence, for the safe operation of DC microgrids, it is imperative to have reliable fault detection and relay coordination scheme. This thesis presents novel fault detection and grounding scheme for DC microgrids. In the proposed fault detection scheme, fault features contained within fault transients are extracted using a multi-resolution analysis technique and are used alongside an ANN classifier scheme for fault classification.

To evaluate the performance, a comprehensive study on the proposed scheme is presented. Simulation based test results asserted that the proposed technique has accurate, fast and intelligent fault detection capability compared to existing DC protection schemes.

Possible improvements to the current technologies and future directions for research, which could enhance the protection of DC microgrids, are also outlined in this thesis.

Keywords— Artificial Neural Networks, DC microgrid protection, Fault detection, Fault localization, Wavelet transform

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DCMG	DC microgrid
RE	Renewable energy
DG	Distributed generator
RES	Renewable energy source
ACMG	AC microgrid
PV	Photovoltaic
EV	Electric vehicle
ESS	Energy storage system
V2G	Vehicle to grid
DWT	Discrete wavelet transform
ANN	Artificial neural network
CB	Circuit breaker
ACCB	AC circuit breaker
HVDC	High voltage DC
MVDC	Medium voltage DC
IED	Intelligent electronic device
di/dt	Derivative of current
FTT	Fast Fourier transform
STFT	Short-time Fourier transform
WT	Wavelet transform
SVM	Support vector machines
ETO	Emitter turn off
MMC	Modular multi-level converter
FCL	Fault current limiter
DCCB	DC circuit breaker

SSCB	Solid-state circuit breaker
IGBT	Insulated gate bipolar transistor
IGCT	Insulated gate commutated transistor
ZSCB	Z source circuit breaker
SCR	Silicon controlled rectifier
SiC	Silicon Carbide
GaN	Gallium Nitride
HCB	Hybrid circuit breaker
FMS	Fast mechanical switch
G-VSC	Grid-connected voltage source converter
MPPT	Maximum power point tracking
SOC	State of charge
BEMS	Battery energy management system
DESAT	Desaturation

1. INTRODUCTION

This thesis presents an effective solution for protection of DC microgrid (DCMG) networks. This chapter covers the background to the research, motivation behind this research, main objectives and thesis overview.

1.1. Background

In recent years, considerable research attention has been given towards renewable energy (RE) supply, to address the environmental issues due to conventional energy sources. Efforts to adopt clean energy sources have resulted in increased integration of distributed generators (DGs) such as solar PVs, micro wind turbines, and fuel cells. However, the increased penetration of DGs to the utility network has resulted in undesirable impacts such as; voltage rise, reduced power quality, protection coordination issues and system stability issues. Therefore, in order to accommodate higher penetration of renewable energy sources (RES), microgrids have become an attractive arrangement due to its controllable, reliable and intelligent energy routing capabilities [1-4].

Microgrid is an active distribution network consisting of DGs, energy storage elements and consumer loads, and is capable of operating either in synchronization with utility grid (grid-connected mode) or in islanded mode. The microgrid networks are capable of functioning autonomously whenever required, to adhere by the economic and operational demands. Microgrids are typically designed to achieve high reliability and uninterruptable power supply capability; hence is an effective solution to supply critical loads such as data center networks. Furthermore, microgrids reduce the energy burden to the conventional power generation and transmission infrastructure [1-5].

1.1.1. DC Microgrids: a Future Power System

DC microgrids are conceptual future power systems to meet the increasing energy demand and solve problems caused by conventional power sources, and are specially researched all around the world.

With the higher penetration of renewable based DG, such as solar PV arrays, together with the increasing use of electronic loads and Electric Vehicles (EVs), have

prompted the idea of using DC distribution systems. Also, with new innovations in the areas of smart homes/buildings, fast EV charging stations, V2G (Vehicle to Grid) technology, hybrid energy storage systems and renewable energy parks, DCMGs are becoming increasingly popular [6-10]. A wide range of traditional DC distribution applications in the fields of telecommunication, traction and vehicular systems can be classified under the DCMG framework and ongoing developments and trends in these fields are largely influential on the development and expansion of DCMGs [10-12]. Figure 1.1 is a representation of a DCMG system with RESs, which can operate in both islanded and grid-connected modes.

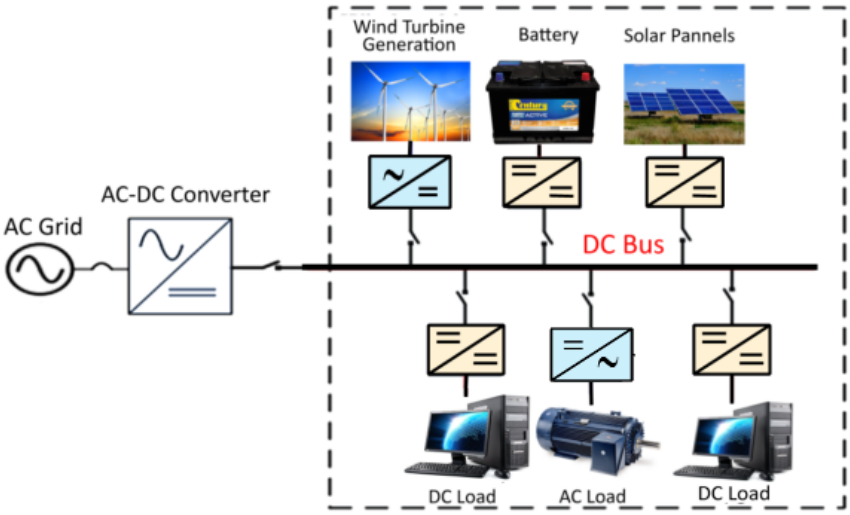

Figure 1. 1 Illustration of a DC microgrid

Advantages of DCMGs when compared to the AC microgrids are given below [7, 10]:

i. DCMGs have the potential to provide more efficient solutions for integrating larger share of RES, improve the reliability, and efficiency of energy transfer.

ii. Provide a natural interface with RESs, electronic loads and most energy storage systems (ESSs) reducing the cost and losses of conversion.

iii. Eliminate the issues with harmonics, synchronizing, phase unbalances and voltage sags to a greater extent.

iv. Requirement for control of reactive power flow is eliminated in DC microgrids.

v. DGs in a DC microgrid do not easily trip against disturbances, meaning DC microgrids have a very good fault ride through capability.

1.2. Problem Statement

The overall function of a DCMG protection scheme is to detect, localize and isolate faults fast and accurately, in order to minimize the effects of disturbances to the supply. The design of the protection scheme depends on a number of aspects, namely the type of faults, which can occur, their severity, the type of protection devices required, primary detection methods, backup protection, measures to prevent faults and measures to prevent incorrect operation of the protection system.

The key challenges associated with DC networks include: the lack of standardization, the unavailability of DC compatible products and protection devices, and topology dependence of protection, protection devices coordination and the relative lack of experience. New simple protection system design with a well defined setting calculation methodology is a crucial requirement for the practical implementation of DCMGs.

1.2.1. Research Gap

Standards for DCMG protection and grounding are not available as of today. Devising a suitable grounding strategy, which could facilitate reliable fault detection, and limit touch voltages to safe limits is important in developing DCMGs as a common power system solution

Although there are certain DCMG fault detection techniques proposed in literature, protection of DCMGs using those techniques is not straightforward due to the following reasons:

- **High sensitivity of network response to fault impedance**- short current rise time imposing strict time limitations for fault interruption.
- **Most techniques rely on communication between devices**- the requirement for multi-terminal measurements, accuracy is affected by sensor and communication errors, high cost of implementation due to additional sensory and communication requirements and requirement of synchronized measurements.
- **The intermittent nature of DGs connected to the network, different loading levels and different modes of operation of microgrids**- changing fault level and changing power flow direction pose challenges to relay coordination.

1.2.2. Main Objectives

The main objective of the research is to design a protection and grounding scheme for DC microgrid systems.

The following specific objectives are to be used to address the above main objective:

1) **To identify the DC microgrid grounding schemes, which could facilitate,**
    - Reliable fault detection,
    - Limit ground fault currents and touch voltages to safe limits
    - Ground fault override capability
2) **To assess the fault characteristics of DC microgrids under different fault events by,**
    - analyzing the transient fault signals using signal processing techniques and,
    - extracting characteristic features
3) **To design an effective protection scheme to detect, localize and isolate faults within safe time limits.**
    - It is hypothesized that signatures in high frequency currents during transients contain information about the disturbances, and it can be used for reliable fault detection and localization.
    - Design involves the use of extracted features with a pattern recognition technique to develop an intelligent and adaptive protection scheme.

1.3.Thesis Overview

The rest of the report is organized as follows:

Chapter 2 presents the literature review covering the area of (i) DC microgrid fault detection and localization, (ii) protection coordination, and (iii) fault interruption equipment.

Chapter 3 presents the development of DC microgrid test system covering the control techniques employed in DC microgrid network. Battery management, current sharing between DGs and other control capabilities of the developed model are evaluated under this chapter.

An in-depth analysis of fault response of DC microgrid network is provided in chapter 4. Individual converter and overall system behavior are investigated here to gain insights into the DC microgrid protection requirements.

Ground fault response of the DCMG network under different grounding configurations is analysed in chapter 5. Design considerations for selecting a grounding arrangement are discussed in this chapter.

The proposed fault detection and localization algorithm is introduced in chapter 6. How the proposed scheme could be incorporated to maintain proper coordination between devices and achieve selective isolation capability also discussed under this chapter. The theoretical basis and methodology behind discrete wavelet transform (DWT) multi-resolution analysis for fault feature extraction is discussed. Step by step approach on how the feature vector is constructed for fault classification is presented under this chapter. Furthermore, the use of artificial neural networks (ANNs) for fault classification is discussed in detail. Different configurations for fault non fault simulations that are used to generate data for ANN training and testing are discussed in this chapter.

Chapter 7 presents the performance evaluation of the proposed fault detection and localization scheme giving a comparative analysis against the existing fault detection techniques.

Finally in chapter 8 conclusions and main contributions are presented identifying the areas of future research.

2. LITERATURE REVIEW

With the new developments in the renewable energy field, DC distribution networks have drawn considerable research attention. More recently, many works of literature on protection schemes and fault interruption equipment have been published. This chapter discusses on various fault detection and localization schemes and fault interruption equipment proposed.

2.1. DC microgrid protection challenges

Developing a network protection scheme is a comprehensive task that involves several challenges [13,14]. Key requirements of DC Microgrid (DCMG) protection and challenges involved are reviewed in this Section. The main protection requirements include, (i) Personnel and equipment safety, (ii) Reliable fault detection capability, (iii) Timely fault detection capability, (iv) Reliable operation with minimum loss of power to the unfaulted sections, (v) Fault ride-through capability under temporary faults, and (vi) Ability to provide backup protection. These requirements must be weighed against the cost of devising a protection scheme [13-18].

2.1.1. DC microgrids faults

Possible fault types of DCMG systems are pole-pole faults and pole–ground faults [15]. Among these, pole–ground faults are the most commonly seen type. Power electronic converters connected to the network may experience internal switch faults that can cause pole–pole faults, which requires the replacement of the device. Pole–pole faults are most often low resistance faults while pole–ground fault can be either low resistance faults or high resistance faults [14,15].

In addition, arc faults can occur at different locations of DCMG, and are difficult to detect due to very high arc fault resistance involved. Faults in DCMG systems can be classified as shown in Figure 2.1.

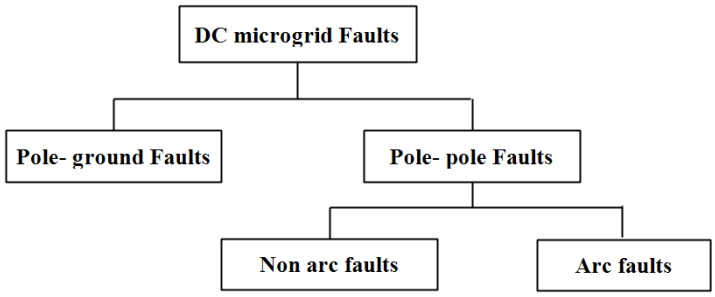

Figure 2. 1 Classification of DC microgrid Faults

2.1.2. Challenges: Fault detection and localization

AC power systems have several protection standards and guidelines, which can be easily adopted for AC microgrids (ACMGs). Contrarily, standards for the protection of DC microgrids are still under development [16]. In addition, unlike for DC systems protection equipment for AC systems are well developed and commonly available.

The absence of effective DC fault detection techniques presents a major barrier against the adoption of DCMGs. Overcurrent and differential elements are used typically for the protection of DC networks in a wide range of applications. However, due to the intermittent nature of DGs connected to the network and different operational modes of the DCMG protection using the conventional protection schemes is not straight forward; changing fault levels and power flow direction impose challenges in fault detection and relays coordination [14, 19]. In addition, it may result in poor fault discrimination and can result in loss of power to the healthy sections of the network. As a result, conventional DC fault protection techniques cannot meet the DCMG protection requirements, and there is a need for the development of fast and accurate DC fault detection scheme [14-20].

Fault localization is required for fast isolation of the faulted zone of the distribution network, and is an essential requirement for quick recovery of the system. Line impedance and traveling wave based techniques have been adopted as an industry standard for fault localization in AC distribution networks [21]. The absence of frequency and phasor information in DC systems prevents the line impedance based techniques to be employed directly [22, 23]. Furthermore, traveling wave based methods for fault localization cannot be employed due to the short lengths of distribution cables.

2.1.3. Challenges: fault current interruption

In AC, the natural zero crossing facilitates the self-extinction of the arc between parting contacts of mechanical breakers. However, in DC, there is no zero-crossing and requires an additional mechanism to force the current to zero [14, 15, 24-26]. In practice, AC circuit breakers (ACCBs) are used for fault interruption in DC networks, with a significant voltage and current derating [27, 28]. In addition, specially constructed mechanical circuit breakers (CBs) with arc chutes are used to dissipate and cool the arc [25]. However, these setups are expensive and require a large space.

Power electronic converters have a limited overcurrent withstand capability, typically in the range 2-3 times nominal load current for few tens of microseconds. Initially, after a fault, DC link capacitors discharges instantly giving rise to fault current with very short rise time and high magnitude. Hence, faults in DCMGs should be detected and isolated, in a timely manner [14, 28]. Due to considerably long operation time of electromechanical CBs (typically longer than 10 ms), they cannot meet the required time limits for DC systems [23, 29]. DC circuit breakers and fault current limiting converters have drawn considerable attention recently as an effective solution for DC fault interruption [30]. However, they are state of the art devices, which incur high costs. Furthermore, considering the high on-state power losses, large volume and weight due to additional cooling requirement, and high susceptibility to transient over-voltages, it is open to question as to whether they offer an effective solution [14, 30, 31].

2.2. DC microgrid fault detection and localization schemes

Reliable fault detection and localization scheme is essential for the safe operation of DCMGs. Compared to the AC networks, DCMG protection techniques are still in its early stage of development. Furthermore, as discussed in Section 2.1, the absence of frequency and phasor information in DC systems prevents the direct adoption of distance protection techniques well-established for AC networks [20, 21].

Existing knowledge on the protection of DC networks in the areas of telecommunication and data center DC networks, MVDC shipboard and traction networks is useful when developing a DCMG protection technique. However,

compared to these networks, fault detection in DCMGs is more difficult due to their smaller scale, several interfacing DGs in DCMGs, multi-terminal nature of the network and high safety requirements. Hence, different protection methods are required for DCMG networks [20].

In designing fault detection scheme for a power distribution network, there are several factors to be considered: (i) fault type, (ii) severity of the fault, (iii) network configuration, (iv) network grounding configuration, (v) safe time limits for fault interruption, (vi) available fault interruption switchgear, (vii) requirement for backup protection and (viii) Preventing false operation of the relays. Furthermore, coordination between component level (eg :- IGBTs), device level (eg: - VSC) and system-level protection schemes should be maintained [13,14, 20, 32].

Different fault detection methods in DCMG networks and their effectiveness are reviewed under the criteria: accuracy of fault detection, ability to localize faults, requirement of additional communication and sensory equipment, cost and ease of implementation.

2.2.1. Overcurrent detection

Overcurrent schemes are generally employed in both AC and DC networks. However, conventional overcurrent schemes for the protection of DCMGs give rise to several protection issues.

The magnitude of fault current in a DCMG depends on network architecture, operating mode of the network (islanded or grid-connected), converters employed to interface DGs, fault parameters and type of fault. Varying fault current magnitude and direction of power flow can cause false operation of overcurrent relays and delayed /non-operation [14, 19, 20]. In [33] a smart relay utilizing the current and voltage magnitude for DCMG fault detection is presented. In this scheme, the relays are built-in with the power electronic converters, and the relays operate autonomously if a fault is detected. If the converter current surpass a preset value and stays above beyond a preset time limit, and at the same time voltage drops below 0.8 pu, a fault is detected by the proposed relaying scheme. In [34], a two-section overcurrent detection technique is proposed for MVDC lines. In this scheme an instantaneous overcurrent threshold is used for primary protection and overcurrent threshold with a time delay for the backup protection scheme. The inability to detect

high impedance faults, and inability to locate the faults, and the absence of selectivity in fault isolation are the major drawbacks of these schemes proposed in the literature.

The use of Intelligent Electronic Devices (IEDs) for fault detection is proposed in [22]. DC Current measurements at IED locations are measured using IEDs are utilized for overcurrent and differential protection. These techniques allow selective isolation of faulty section without interrupting the supply to the healthy parts of the network. Furthermore, differential protection enables high impedance fault detection capability. In [35], a similar technique using IEDs is presented, where current magnitudes, direction and bus voltage levels are monitored by IEDs at different locations for fault detection.

2.2.2. Derivatives of current

Use of rate of change of current (di/dt) for quick detection of DC faults is investigated in [20]. The fast discharge of the DC converter capacitors results in high magnitude fault current with a short time constant. This transient current is damped by fault current loop impedance. To prevent the total discharge of network capacitors following a fault, a fast fault detection method is required. Hence, di/dt based protection schemes are deemed suitable for DC networks compared to other schemes due to its fast fault detection capability [20, 36].

In [37], fault detection technique utilizing the initial di/dt value is presented. This fault detection technique based on initial value of di/dt utilizes initial response of DC network capacitance to a fault for detection of faults, and to estimate the location of the fault. Similar initial response for both low and high impedance fault was observed in this study, hence allows the identification of faults unaffected by fault impedance. However, under high impedance faults, di/dt decays fast compared to during low impedance faults. Analyzing the initial di/dt response allows the detection of high impedance fault situations [37]. Although di/dt schemes facilitate very fast fault detection, the detection accuracy of this technique is gravely affected by measurement noise and disturbances in the network [19, 20, 37].

2.2.3. Differential protection

Differential protection can be used to protect predefined zones of protection in the network. The existence of DGs, varying load conditions resulting in different fault current levels and changing power flow direction has no impact on differential

schemes; hence, offer a reliable protection solution for both AC and DC networks [14, 19, 22].

In [38], differential protection scheme with master controller and two slave controllers for each protection zone is proposed. The currents at the both ends of the protection zone are measured by the slave controllers, and are communicated to the master controller. In the event of a fault, the difference of current magnitudes at either ends of the protected element differs allowing the fault to be detected by the master controller.

Differential techniques depend on communication of devices monitoring line current at the two ends of protective zone. Hence, considering the communication time delay between devices, and maintaining proper synchronization among devices is important when designing a differential protection scheme for the network.

2.2.4. Distance protection

AC networks employ distance protection schemes for the localization of faults in the network. However, frequency information are inherently absent in DC systems, which prevents the direct adoption of these distance protection schemes in DC networks. Furthermore, during a fault transient in a DC network, voltage and current waveforms oscillate rapidly and frequency varies; hence, it is difficult to define a fundamental frequency [14]. In [39, 40] novel technique for the network parameter calculation in order to determine the DC network impedance under a defined frequency is proposed. This allows the detection of faults, and distance to the faults using the distance protection principles.

In [39], the impedance estimation scheme, which does not require an external signal injection source, is proposed. A distance protection scheme using active impedance measurement for DC shipboard networks is proposed in [40]. In this proposed scheme, a wide frequency current signal is injected and the resulting voltage is measured to determine the equivalent network impedance to be used with the distance protection scheme.

2.2.5. Signal processing based detection schemes

Fast Fourier transforms (FFT) is less useful in analyzing a dynamic signal due to the absence of time scale information. Hence, the use of FFT for power system signal processing applications is limited [41].

Short-time Fourier transform (STFT) analyses signals in both time and frequency domains, and is a widely employed tool for power system signal processing [41, 42]. The use of STFT for quantitative analyses of high frequencies during a fault transient in DC network is discussed in [43]. However, achievable time and frequency resolution using the STFT is limited due to constraints on the selection window size. Narrow time window will give good time resolution at the expense of frequency resolution. On the other hand, a wide time window will result in good frequency resolution but poor time resolution [14].

Wavelet transform (WT) analyses a signal in both time and frequency domains under multiple resolutions. Hence, compared to STFT and FFT techniques, WT is capable of giving better time and frequency resolution of the signal; hence is popularly used for signal processing applications. Wavelet representation of a signal provides a good representation of the time variation of the frequency contained within the signal. Wavelet multi-resolution analysis techniques have been used for wide range power system applications, including network fault detection and recognition of transient events [44-57].

The common methodology for the use of wavelet transformation for fault detection is to extract the unique features of fault signal using wavelet decomposition, and to use these quantified features as variables with an algorithm to determine fault situations [14]. Literature discuss different techniques to capture these characteristic features. One technique is to compute and compare the magnitude of detail coefficients to identify characteristic changes in the signals [45]. However, employing raw wavelet coefficients values for fault detection requires large memory space and computing time. In [41], wavelet decomposition based fault detection technique for medium voltage (MV) shipboard networks is presented. This method uses the energy variations in different decomposition levels to identify characteristic changes in the signal during the fault in the network. This reduces the required memory space and processing requirements for fault detection. In addition, the use of several statistical parameters for fault feature identification from the wavelet decomposed signal is discussed in the literature [45, 47].

2.2.6. Pattern recognition schemes

Recently, data-driven pattern recognition techniques have garnered continuous interest, especially for power system applications. Not having to define hard thresholds is a major strength of fault detection techniques based on pattern recognition. It helps in intelligent and accurate fault detection unaffected by changes in the network conditions.

Artificial neural networks (ANNs) have been tested for fault classification in AC, HVDC and MVDC networks, and have demonstrated that they are fast, accurate and robust in its performance [47-53]. The ANNs are required to be trained using fault data obtained under different network operating conditions, fault types and fault locations to ensure correct fault detection unaffected by fault parameters and changes in the network. These pattern recognition based techniques have shown a vast potential in several fields of engineering applications and shows promising results in several power system protection applications.

2.3. DC microgrid protection coordination schemes

Coordination among protection devices is essential for minimizing fault clearing time, facilitating fast restoration of power and to minimizing power outages in the network. Differential fault detection techniques with bounded zones of protection are proposed in [22, 38]. However, these schemes are incapable of providing backup protection to the adjoining protection zones. This is a major drawback associated with these protection coordination schemes.

Primary protection relays operates as the main protection relay for a component or bounded zone of the network. Backup protection relays are required to operate in the events of primary protection relay or breaker failures. The protection coordination method is selected based on protection methods deployed, fault clearing time limits, ability to distinguish between temporary and permanent faults, and ability to ride-through fault events [14].

The commonly used protection coordination methods employed in DCMGs is through relay time grading and communication between relays, and is discussed in the sections below.

2.3.1. Protection coordination: time grading of relays

In time graded relays, relay operating times are set in a way primary protection relays protecting the faulted section operates first. Relay time grading requires the backup relays to operate, if the primary protection fails [14].

The coordination method between fast-acting fuses and circuit breakers for coordinated protection of DCMG is proposed in [54]. Fast-acting fuses placed at selected locations of the network is capable of fast fault clearance, and compared to circuit breakers is cost effective. Time graded overcurrent relays built into circuit breakers are positioned to isolate zones/components of the network in case of a fault.

Protection coordination scheme among fuses, relays and converters with fault current limiting capability is presented in [33]. Fast-acting fuses are employed as the main protection device within the AC zones of the network. Fast-acting relays, which act faster than the fuses are used to clear faults in the DC side, thereby avoiding the blow off of fuses for DC side faults in the network.

2.3.2. Protection coordination: communication based

Coordination between relays based on communication among relays is a reliable solution for DCMG systems. In [22] Intelligent Electronic Devices (IEDs) are positioned at selected locations of the network, and inter device communication method is used to keep the coordination between these devices. A similar relay coordination approach is presented in [10], where voltage and current waveforms monitored at relay locations are communicated between relays to determine occurrences of faults and fault locations. A reliable communication channel is important for protection coordination; hence, is affected by failures in the communication channel, and communication delays should be accounted for.

2.4. DC microgrid fault interruption

To ensure safe operation of distribution networks, appropriate fault interruption equipment are required, either to interrupt fault currents or to isolate faulty sections in the network. As discussed previously, DC networks impose stringent requirements for interrupting fault current. Fast fault current rise requires the fault to be interrupted within a very short time span. Furthermore, the absence of natural zero crossing in the DC current requires fault interruption switchgear to force the current to zero using an alternate method. Hence, DC compatible interruption devices are required,

which can operate very fast, and with a special assembly for DC current breaking [14, 20, 22, 23].

In [20, 23], fault current interruption time limits for a voltage source converter (VSC) based DC networks are assessed. Preventing transient over-voltages during fault interruption, fault detection time, power losses within the breakers, implementation cost, coordination between protection devices and continuity of supply to the healthy sections are important factors to be considered in the selection of switchgear for DCMG network.

2.4.1. Converter fault current blocking and current limiting techniques.

Power electronic converter architectures with fault current blocking capability are commonly employed in HVDC networks and MVDC shipboard and traction networks. They are capable of quickly blocking the currents through converter controls. In practice, IGBT converters are embedded with IGBT self-protection schemes (both overvoltage and overcurrent), which activates under fault conditions [55, 56]. However, with IGBTs blocked, in conventional converter architectures, such as two level VSCs and DC-DC buck/boost converters, the fault currents will start to flow through freewheeling diodes. These diode freewheeling currents will only be limited by cable and fault impedances. It is not possible to achieve converter blocking with conventional VSC and DC-DC converters, and specially constructed converters with current blocking ability are required [14, 20, 57].

Under normal operation, power electronic converters are capable of limiting maximum current flow. However, most of the conventional converter models cannot limit fault current due to the existence of freewheeling diodes. In [57-64], specially designed converter model with current limiting ability when a fault in the network is detected is presented. These fault current limiting converter architectures employ multi-mode control schemes, which change the control parameters to limit current flow through the converter when a fault is detected. Current limiting converters work in coordination with other protection devices to minimize the damages to the network by fault current, and to prevent loss of power for prolonged periods during temporary faults. Loss of supply to the whole network including the healthy sections of the network is a major drawback of this method [14]. Fault current blocking converter architectures proposed for DC networks are presented below.

1. ETO thyristor converter architectures

Replacing the freewheeling diodes of conventional IGBT based VSC architecture by ETO thyristors is proposed in [33], to enable current blocking capability. In these converters, converter does not provide a diode freewheeling path for the fault current to flow, as in IGBT converters. The converter architecture is shown in Figure 2.2. The ETOs have a high current and voltage handling capability. In addition, they have lenient switching requirements compared with IGBTs. Once a fault is detected, soft shut-down method is employed, where the ETO gate voltage is gradually reduced to prevent transient over-voltages during current blocking [33, 57, 58].

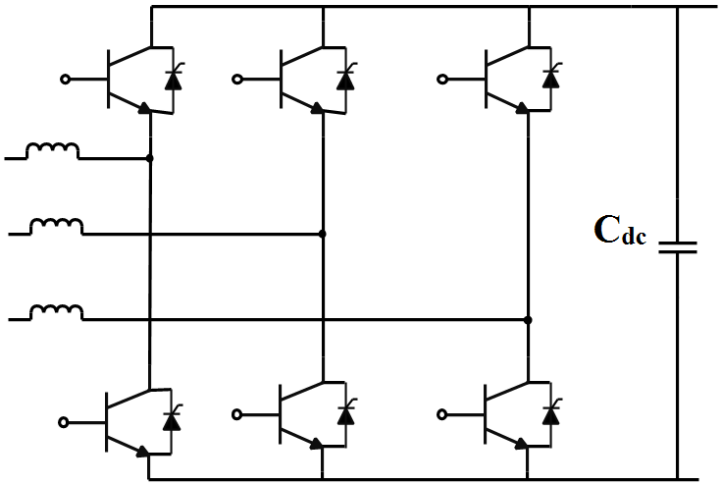

Figure 2. 2. ETO thyristor based VSC architecture.

2. Back-to-back VSC converter architecture

Back-to-back VSCs (see Figure 2.3) feature voltage and current regulation capability on both sides of the converter. In addition, this converter is also capable of blocking fault currents during a fault on either side [59, 60].

Back-to-back converter architecture uses two active VSCs; hence, increases the cost and converter size. The presence of two conversion stages also increases the power losses associated with the converter.

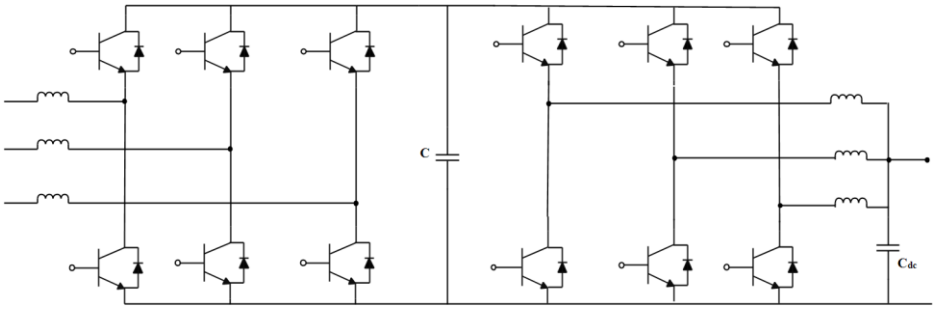

Figure 2. 3 Back to back VSC architecture

3. Isolated DC-DC converter

DC-DC converter architectures based on isolation transformer, which is capable of controlling/blocking current during faults are proposed in [59, 62-64]. Dual active bridge (DAB) converter architecture based on two full-bridge converters through a high frequency transformer is shown in Figure 2.4. In addition, DAB based isolated DC-DC converters are capable of limiting fault current on both sides of the DAB [15, 59].

The literature discusses several modular multilevel DAB architectures for both high and medium power applications [59, 61, 65]. However since they require a high number of power electronic switches and have several conversion stages, modular multilevel converters are conventionally used in HVDC networks and are less cost-effective with LVDC and MVDC networks [14]. Recently developed wideband gap (WBG) devices (eg:- silicon carbide (SiC) and Gallium nitride (GaN)) with their low on-state losses and other favorable traits presents a possibility to fully utilize the abilities of these converter architectures for LVDC and MVDC applications [15,66,67-69].

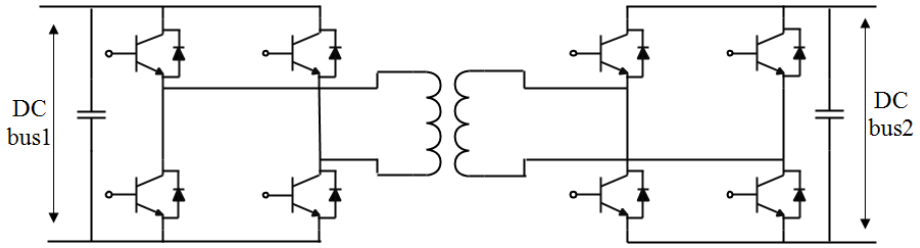

Figure 2. 4 DAB architecture with DC fault current limiting capability

2.4.2. Fault current limiters (FCLs)

Fault current limiters (FCLs) can be utilized in DC networks to limit fault currents when a fault is detected [70]., FCLs have a zero impedance under normal operation, and. internal impedance increases once a fault is detected, in an effort to limit fault current flowing through the FCL. The strategic placement of FCLs for the protection of distribution networks is studied in [70, 71]. These studies show that the point of connection of DGs to the power network is the optimum position to connect the FCL for fault current limitation.

The connection of protective inductors at power electronic converter terminals to limit current transients within HVDC networks is studied in [72]. However, the requirement of a large iron core, which as a result increase the size, weight and cost of installation, is the main drawback of this technique. Furthermore, this FCL arrangement is only capable of limiting time varying currents and is not effective during steady fault currents.

The FCL technology based on superconductor materials is discussed in [74-75]. These FCLs operate as a superconductor under normal operating conditions and when the current reaches a critical level, it changes the superconducting state to increase the resistance, thereby effectively limiting the current. Design criteria and selection of parameters for superconductor based FCLs considering the power network requirements are presented in [73]. One of the main disadvantages of FCLs is the requirement of long lengths of superconducting materials; hence FCLs are large, heavy and expensive.

Solid-state FCL designs for DC networks are presented in [76, 77]. Smaller size, fast response times and enhanced control capabilities are major advantages associated with solid-state FCLs. However, solid-state FCLs have a high conduction loss, which is a main drawback.

2.4.3. Fault current interruption with DC side circuit breakers

DC fault current interruption techniques using DC CBs have been discussed in [23,28,78,79]. These techniques offer selective fault interruption capability, allowing zones of the network unaffected by the fault to continue operation.

As discussed in Section 2.1, due to the absence of a zero-crossing in the DC current waveform, breakers face a unique challenge of no natural method for extinguishing the arc that occurs during current breaking.

The use of reactors in series with the conventional ACCBs to interrupt DC fault current is discussed in [78]. Due to the mechanical constrictions, ACCBs cannot meet the time limits for fault current interruption in DC networks. Regardless of the fact that AC breakers being a mature technology offer advantages such as low cost, DCCBs are a better solution for DC networks as they can achieve timely DC fault isolation. Several DC breaker designs; mechanical, solid-state and hybrid (solid-state and mechanical) have been proposed and developed recently for DC applications ranging from LVDC, MVDC and HVDC.

1. Mechanical DC breakers

Mechanical DC breakers are based on the principle of resonance, where oscillation circuits are employed to create a zero-crossing point artificially. In Figure 2.5 mechanical DCCBs circuit with passive (Figure 2.5(a) and active (Figure 2.5(b) commutation circuitry are shown [24, 80, 81]. Mechanical DCCBs comprises of a mechanical switch and resonance circuit for force commutation. In addition, metal oxide varistors (MOVs) are used to absorb energy during the current interruption. When a fault is detected the mechanical switch is opened and the current is commutated through the commutation circuitry. The resonance circuit (capacitor and inductor arranged in series) creates an oscillating current, and creates a zero-crossing point between contacts of the mechanical switch. Then mechanical switch can open at zero current [15]. Mechanical DC breaker response time is much slower (~30 ms) than DC link capacitor discharge due to mechanical constrictions. Hence, the network has to undergo high fault current transient, during a fault before the fault is interrupted.

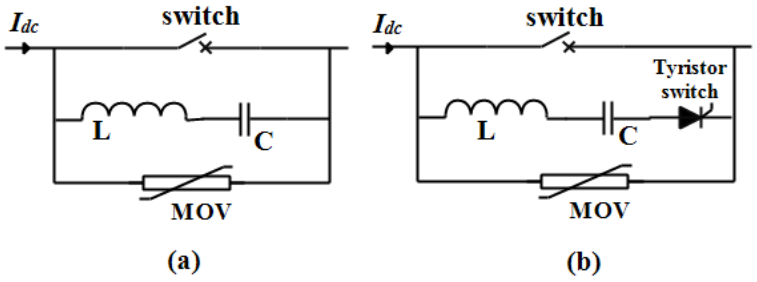

Figure 2. 5 Mechanical DC breakers with (a) passive commutation, (b) active commutation circuit.

2. Solid-state circuit breakers

Solid-state circuit breakers (SSCBs) offers a promising solution for DCMG fault interruption with its fast current breaking and high constant current handling capability compared to other devices. The literature discusses several SSCB designs based on, ETOs, GTOs, IGBTs and IGCTs for DC current breaking [14, 15, 28].

Modified SSCB assembly with bidirectional power flow capability is shown in Figure 2.6. The proposed breaker design uses a string of series connected solid-state switches in order to handle the transient voltages safely during the current interruption, and prevents the transients exceeding the withstand levels of the power electronic switches. IGBTs are often the common choice in these breaker designs because of wide commercial availability and fast response capability. However, for high power applications, IGCTs are preferred over IGBTs due to their low conduction losses and rugged structure [28].

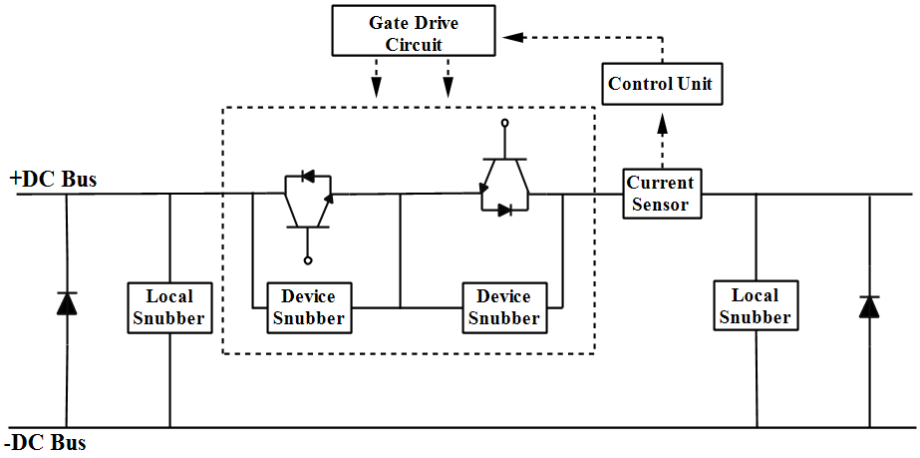

Figure 2. 6 Solid-state circuit breaker assembly.

Figure 2.6 shows the SSCB design, which provides the functionality of the complete CB assembly. Fault detection is carried out by the breaker controls scheme itself; hence, external fault detection relays are not required. When a fault, occurs

the control unit signal the gate drive circuit and turns off IGBT switches. Snubber circuit and freewheeling diodes dissipate the energy during the current breaking [24,28,82].

In this SSCB design, solid-state switches must be actively driven OFF before current level exceeds the interrupt capability of the power electronic switch. Hence, fast fault detection within the time limits is a necessity. To overcome these limitations, Z source circuit breaker (ZSCB) design (see Figure 2.7) is proposed in [24]. Unlike the SSCB, ZSCB absorbs part of the large transient fault current to create a current zero-crossing. Silicon control rectifier (SCR) is naturally turned off once the zero-crossing is created. Natural commutation of the solid-state switches facilitates the fault to be isolated, without having to force commutate. In addition, passive elements used in ZSCBs limits the peak current within the solid-state devices. Hence, these are not required to withstand high currents.

The ZSCB design proposed in [24] has some drawbacks, such as the inability to protect against overload conditions and only being able to interrupt faults with high fault transients. In addition, for less severe faults, fault current transient energy may not suffice for natural commutation. ZSCB design which, adopts a separate force commutation circuitry is proposed in [83]. In addition, ZSCB circuitry has been modified to achieve bidirectional power flow capability in [60].

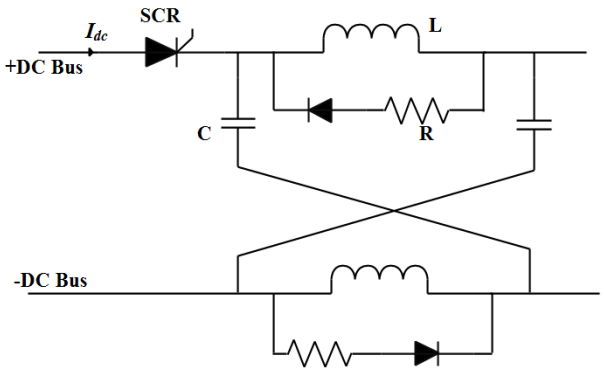

Figure 2. 7 Z source circuit breaker circuitry

Although SSCBs devices offer a feasible solution of DC fault interruption, they mostly rely on additional sensing, processing and control. Furthermore, they employ additional cooling systems, and incur considerable power losses at solid-state device junctions. The capability to use SiC and GaN wideband gap devices to address the

issue of losses at semiconductor junctions has been investigated [15,24,83,84]. It is presumed the performance of SSCB technologies to be improved by using WBG device technology.

3. Hybrid CBs (HCBs)

Hybrid CBs (HCBs) is an alternative to address the issue of high conduction losses of SSCBs, HCB is a combination of SSCB and bypass branch, which consists of commutating switches in series with fast mechanical switch (FMS) as shown in Figure 2.8. Under normal operation, current flows through the bypass branch of the HCB [85-90]. When fault current is detected, the commutating switch is turned OFF to pass the current through the branch of SSCBs. This allows the FMS to be opened at zero current. Then the current through the SSCB branch is blocked by the SCCB assembly. Possible transient interrupt voltage during fault interruption is handled by MOVs. The MOVs also absorb inductive energy in the line following the current interruption. Practical realizations of HCBs are discussed in [86-89].

In this setup low voltage commutating switches are adequate to commutate current to SSCB branch; hence, low conduction losses are incurred. Due to the very short ON state, solid-state devices do not require additional cooling, allowing HCBs to be built at low cost and compact compared to SSCBs. Although HCBs provide advantages of both mechanical and solid-state breaker technologies, due to mechanical constrictions, HCBs have relatively slow operating speed compared to SSCBs (typically between 500 μs-2 ms) [14, 31, 90].

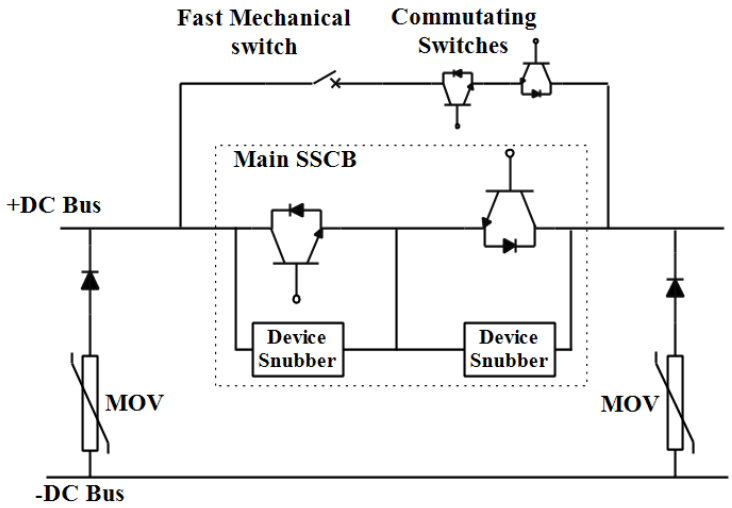

Figure 2. 8 Hybrid circuit breaker circuitry

2.5. DC microgrid modeling, control, experimental setups and standardizations aspects

An increasing number of research work on DCMG have been carried out, covering application in the area of smart DC homes/ buildings, EV charging stations, transit networks, and telecommunication networks. When designing a DCMG key issues to be considered are; (i) swift current sharing between RESs, (ii) achieving economic and autonomous operation, and (ii) catering the intermittent nature of RESs to maintain reliable power supply.

2.5.1. Overview on DC microgrid architectures

Driven by the practical requirements, several DCMG topologies have been proposed. The criteria considered are, system reliability, robustness and control flexibility. As these criteria are often conflicting with each other, different compromises are taken into account when deciding the most suitable microgrid configuration for a particular application [4, 91-93].

1. DC microgrid network topologies

A number of DCMG network topologies are reported in the literature and some of the most common configurations are assessed in this Section.

For the purpose of our study, the topologies of DCMGs are classified into four categories: (i) Radial configuration, (ii) Ring configuration, (iii) Mesh configuration and (iv) Zonal type configuration and are shown in Figure 2. 9 [5, 94, 95]. While radial network topology has simpler control requirements, more complex network architectures such as ring, mesh and zonal topology provide better operational reliability and flexible control capabilities. However, main drawback when of complex network topologies are: high cost of implementations, complex power flow management and relay coordination issues.

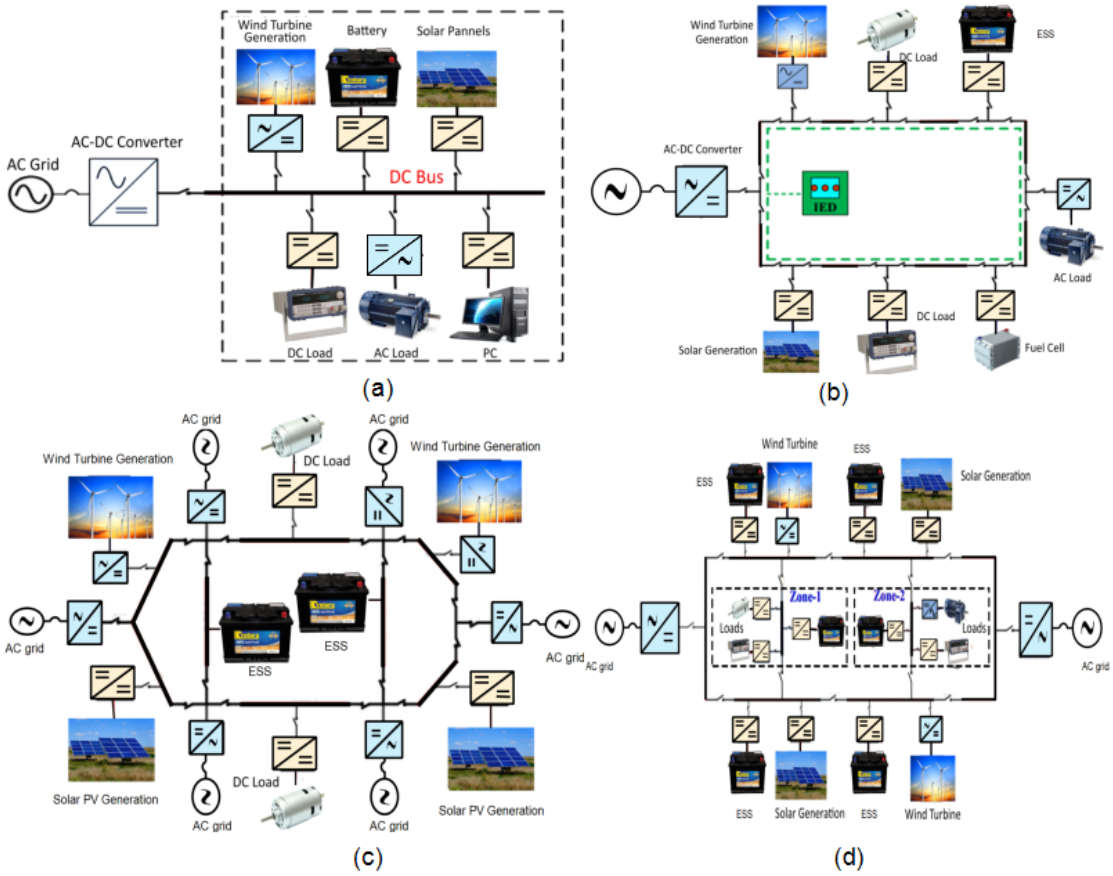

Figure 2. 9 DC microgrid with (i) Radial configuration, (ii) Ring configuration, (iii) Mesh configuration and (iv) Zonal type configuration

2. *DC microgrid voltage polarity*

The power in the DCMG system can be transmitted using two-wire (unipolar) or three-wire (bipolar) system. The difference between unipolar and bipolar DC systems is the number of selectable voltage levels [94, 96, 97].

A. *Unipolar DC microgrid system:*

In the Unipolar DC system, sources, converters and loads are connected between two wires. The positive and negative pole of the DC bus as shown in Figure 2.10 (a). Since energy is transmitted over the DC bus at one voltage level, the selection of that voltage level is based on the requirement of the end-user. Proper selection of voltage level can decrease the number of DC-DC converters connected to the network. The main concern in the selection of the voltage level is that, with low voltage level, the transmission distance is limited while the high voltage level increases the safety risks [94, 97].

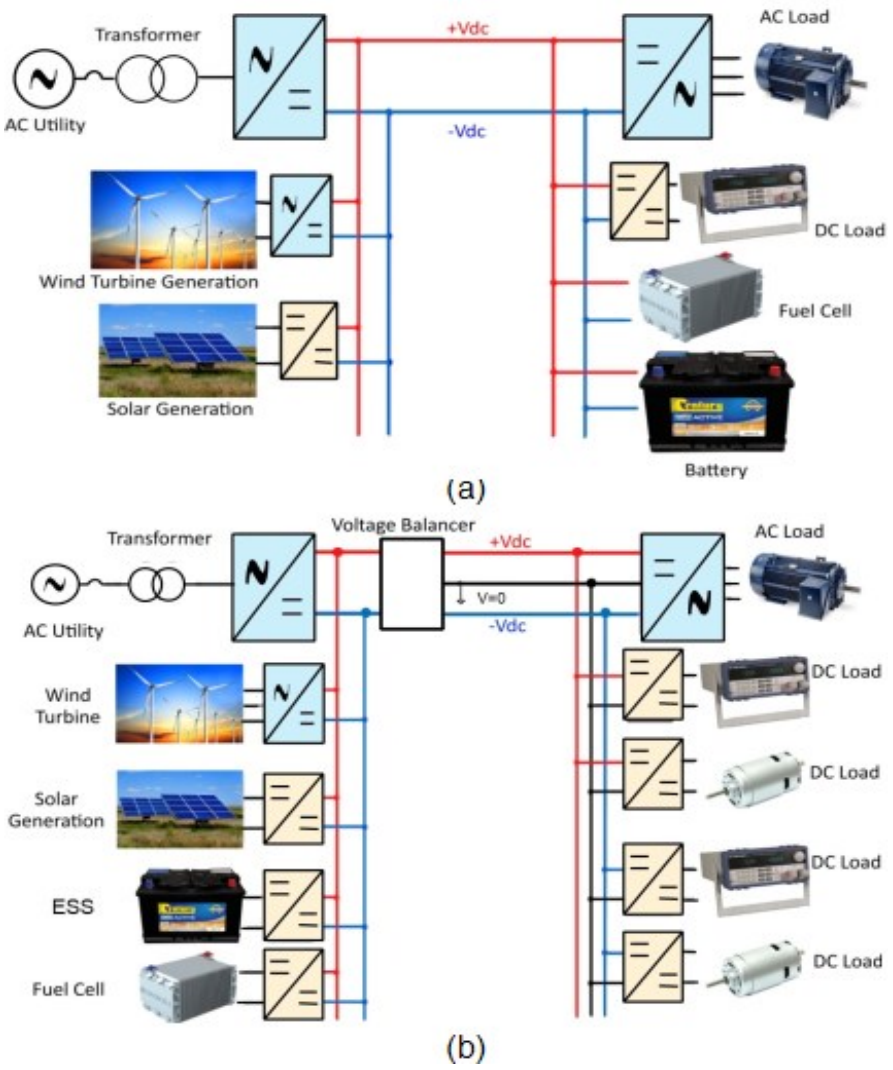

Figure 2. 10 DC microgrid with (a) unipolar DC bus, (b) bipolar DC bus

B. Bipolar DC microgrid system

The bipolar DC system can overcome the above mentioned limitations of the unipolar system. The bipolar DC system consists of $+V_{dc}$, $-V_{dc}$ and neutral line as in Figure 2.10 (b). Consumers have the option to choose between three voltage levels $+V_{dc}$, $-V_{dc}$ and $2V_{dc}$. This decreases the number of DC-DC converters required to connect loads to the microgrid. A bipolar system offers more flexibility towards different loads. For example, ESSs can be connected to a one pole together with loads requiring high reliability. Furthermore, all renewable energy sources (RESs) can be connected to one pole with loads that should only be run when there is enough power [94, 95, 97].

3. AC grid interface of DC microgrids

The interface between DCMG and AC utility grid is important as it determines how electrical power flows between AC and DC networks. In modern DCMGs, AC grid interface is designed to facilitate bidirectional power flow allowing the excess energy generated by RESs to be transferred back to the AC grid. There are several AC-DC converter topologies discussed in literature covering both unidirectional and bidirectional power converter topologies. In some DCMG architectures multiple parallel AC-DC converters are used to increase the reliability and flexibility of the supply. These different interfacing AC-DC converter topologies have a significant impact on the selection of the DCMG architecture, control strategy, grounding and protection schemes.

Two-level Voltage Source Converter (VSC) with Active Front End (AFE) filter is a commonly used AC-DC converter topology in DC distribution systems [94, 98, 99].

2.5.2. DC microgrid Control requirements

Renewable energy sources (RESs) connected to a microgrid system, such as solar PV and wind follow the meteorological conditions, while loads operate according to their own profile. This intermittent behavior urges controllable sources such as Energy storage system (ESS) and AC grid interface converters to accommodate the variable demands and balance the power.

Unlike AC microgrids, the control of DCMGs is much simpler in the sense that they do not require reactive power control, and only the voltage control is required. The system voltage is dependent on active power flow. In order to ensure the stability of the system, the active power flow within the DCMG must be balanced at all times ensuring DC voltage be maintained at the required level [100].

The main control objectives of a DCMG include

1) Regulating bus voltage and maintaining stability.
2) Efficient power sharing between interlinking converters, DGs, loads, other microgrids and external grid networks.
3) ESS management.

4) Energy management during the grid-connected and islanded mode of operation.
5) Response to faults in the network.

DC microgrid stability refers to the ability of the system to maintain steady bus voltage and current sharing among DGs and loads after being subjected to a disturbance [101]. The stability of the DCMGs can be an important issue under high penetration of load converters, which behaves as constant power loads [102,103].

2.5.3. DC microgrid control hierarchy

The control of microgrids interfacing DGs has been extensively studied in the last few years. Several microgrid control architectures have been proposed in the literature [104-109].

Decentralized or centralized control using droop schemes are conventionally adopted in microgrids. However, with conventional droop control, there are inherent drawbacks of current sharing and voltage deviations. In addition, the microgrid is incapable of achieving a globally optimal control performance. To cope with these drawbacks, hierarchical control schemes were adopted [109,110]. With the increase of DGs connected to the network and complexity of the network, to achieve multiple control objectives, hierarchical control and energy management schemes have become essential.

The control of DGs in a DCMG can be achieved using different control architectures. Several such DCMG control architectures have been discussed in the literature. Five different control architectures, which can be categorized as: (a) Centralized control [104,105], (b) distributed autonomous control [106], (c) master-slave control [107], (d) multi-agent based control [109], and (e) hierarchical control, are discussed in literature. Among these decentralized control has advantages over other methods due to less reliance on communication, more autonomous and flexible control structure. Conversely, other control architectures are capable of providing better voltage control and current sharing among network DGs, compared to decentralized architecture. The choice of DCMG control architecture can vary according to the application (residential or commercial), or other features, such as size, topology, and location.

1. Centralized control

All available measurements of the considered microgrid are gathered in a central controller that determines the control actions for all units. The main advantage of centralized control is the central controller receives all available information, allowing it to achieve a globally optimal control performance. However, this method inherits several disadvantages including, heavy computational burden to the central controller, reliance on communication and not being scalable.

2. Decentralized control

Control architecture without any form of communication between local controllers. Mostly implemented as a droop control scheme (see Section 2.5.4), which uses droop characteristics that adjust active power output with locally measured DC voltage. This control architecture is capable of operating when all communication channels fail. However, optimal operation of the DCMG is rather difficult due to the lack of information to local controllers.

3. Master-slave control

In this architecture one converter is selected as the master unit that operates in voltage control mode, to maintain nominal bus voltage. Other converters are configured as slave units to operate in the current control mode. In [107] master-slave control scheme relying on communication between devices is discussed.

4. Multi-agent based control

Multi-agent based control architecture is composed of multiple agents which communicate with each other cooperatively. Multi-agents have the capability to operate in an autonomous and intelligent manner. In this architecture, all local agents are equally important and can communicate with each other agents. Local agents act upon received information and in cooperation with each other, to achieve the globally optimal operation of the DCMG. Algorithms based on gossiping and consensus algorithm are commonly used for communication between agents. In this architecture, single point failure is absent, and also when a single communication channel fails the required information can still reach the necessary agents, via other agents. Hence, it is a robust control architecture.

5. *Hierarchical control*

Hierarchical control endows smartness and flexibility to the network and it is capable of achieving multiple control objectives and optimal operation of the DCMG [109-110]. In hierarchical control structure, multiple objectives do not affect each other.

A three-level hierarchical control structure is shown in Figure 2.11.

The objectives of each control levels include;

1. *Primary level*- Adjust the voltage reference for the inner current and voltage control loops to ensure normal and stable operation of converters connected to the microgrid.
2. *Secondary level*- external common controller for the restoration of voltage and current deviations in the microgrid.
3. *Tertiary level*- optimal operation of DCMG in system level. This level of control regulates the bidirectional power flow between the microgrids and the external grid.

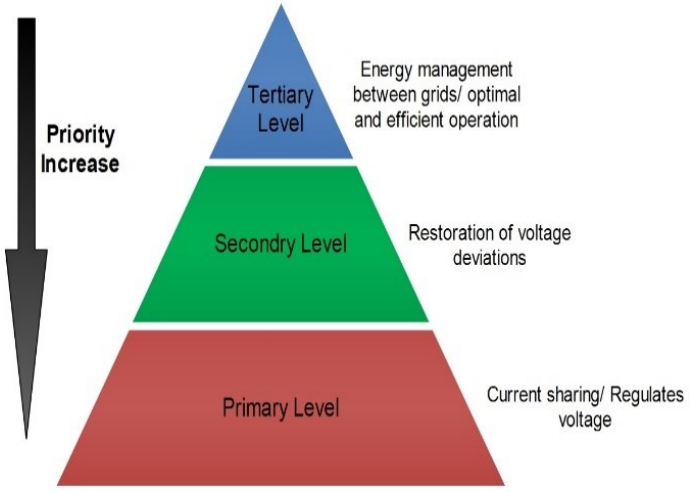

Figure 2. 11 Hierarchical Control levels for DC microgrid system

A. Primary control level

Primary control is the first layer in the hierarchical control scheme shown in Figure 2. 12. It is responsible for local voltage and current control, in order to meet the power sharing requirements of DGs and maintain the bus voltage stability. Decentralized control methods are adopted mainly in this control level, and mainly focus on the stable operation of the network and power sharing between DGs and

loads. Typically droop control schemes are employed for power sharing between DGs (See Section 2.5.4).

In a typical droop control scheme, droop coefficient, $\boldsymbol{R_D}$ is employed. The output voltage, $\boldsymbol{V_o}$ is determined by output current, $\boldsymbol{I_o}$ and the droop coefficient, $\boldsymbol{R_D}$ as shown in (2.1).

$$\boldsymbol{V_o = V_{DC}^{ref} - I_o R_D} \qquad \textbf{(2.1)}$$

Here, $\boldsymbol{V_{DC}^{ref}}$ is the DC voltage reference at open circuit conditions.

B. Secondary control

Generally, droop control and its variants, and DC bus voltage signaling control schemes are used in primary control. However current sharing and bus voltage regulation issues still exist. A secondary controller (upper level control structure) is adopted to address these issues [6-7, 19].

As it is discussed, current sharing and voltage regulation between DGs, ESSs and loads are achieved by the primary controller with no communication link between controllers. To achieve improved control, a secondary control level which sets the reference parameters to the primary control is introduced (see Figure 2. 12). The main control objectives of the secondary controller are to minimize bus voltage deviations caused by primary control, achieve improved current sharing and power flow optimization [110].

As shown in the Figure 2. 12 voltage regulation factor, δV_o is introduced by the secondary controller to achieve the improved output voltage V_o. Then, (2.1) can be rewritten as (2.2):

$$\boldsymbol{V_o = V_{DC}^{ref} - R_D i_o + \delta V_o} \qquad \textbf{(2.2)}$$

Voltage regulation factor $\boldsymbol{\delta V_o}$ can be expressed as (2.3)

$$\boldsymbol{\delta V_o = K_p\left(V_{DC}^{ref} - V_{DC}\right) + K_i \int \left(V_{DC}^{ref} - V_{DC}\right) dt} \qquad \textbf{(2.3)}$$

Where $\boldsymbol{Kp}$ and $\boldsymbol{K_i}$ are control parameters of the tertiary control compensator.

To achieve the secondary control, a communication link between controllers is required. The literature discusses different secondary level control schemes to realize DC bus voltage regulation. Furthermore, it should be noted that primary control level

functions as the main controller of DC bus voltage. Secondary controller accommodates bus voltage deviations through regulation of $\boldsymbol{\delta V_o'}$, which is input into the primary control structure, and does not actively take part in bus voltage control. Hence, DC bus voltage hunting effect does not occur in this control structure.

C. Tertiary control

The control objectives of tertiary control include efficient operation, energy management, and optimal power flow. Tertiary level control scheme adjusts the set points for the secondary control scheme to achieve the above objectives [109, 110].

Energy management between DCMG and other stiff grids or microgrids is achieved by tertiary control [109, 110]. As shown in Figure 2. 12 by measuring the current $\boldsymbol{I_G}$, it can be compared with the current reference, $\boldsymbol{I_G^{ref}}$. The current reference takes positive or negative value depending on whether we want to import or export energy.

Voltage regulation factor $\boldsymbol{\delta V_o'}$ can be expressed as in (2.4),

$$\boldsymbol{\delta V_o' = K_p^T\left(I_G^{ref} - I_G\right) + K_i^T \int\left(I_G^{ref} - I_G\right) dt} \qquad \textbf{(2.4)}$$

Where $\boldsymbol{K_p^T}$ and $\boldsymbol{K_i^T}$ are control parameters of the tertiary control compensator.

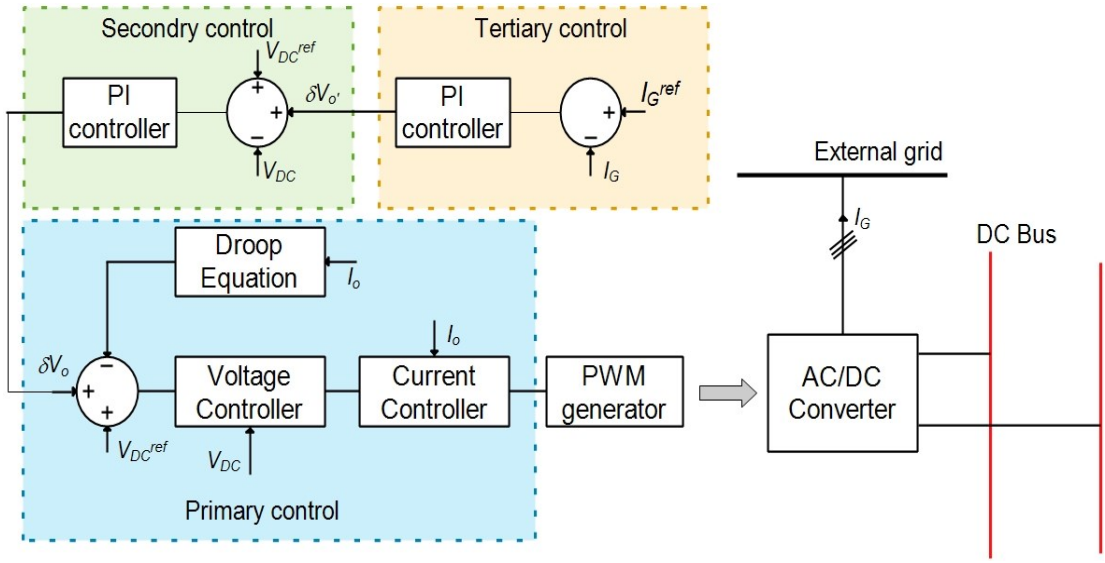

Figure 2. 12 Three level hierarchical control structure for DC microgrid.

2.5.4. Load power sharing methods/ Primary control methods

Although distributed and decentralized control architectures offer a satisfactory level of control performance in small networks, for more complex and clustered networks, it requires more intelligent control process. The hierarchical control structure is thus becoming a standardized control structure for microgrids. As discussed in Section 2.5.3, primary control involves voltage/current regulation and power sharing between local DGs. Droop control and DC bus voltage signaling based control schemes are utilized as the primary control technique in DC networks and is discussed below:

1. Droop control

Droop control and its variants are the commonly used control methodologies in integrating several DG sources to a DCMG. The droop control method is a decentralized voltage control method in which each output voltage reference is controlled based on its output current [111]. Droop control is realized by reducing the output voltage as the output current increases or vice versa to compensate for the mismatch of power flow. This allows the parallel connected converter operation even in the absence of a communication link. Literature discuss three basic types of droop control methods, namely (i) conventional droop control [112], (ii) nonlinear droop control [113,114] and (iii) adaptive droop control [111].

A. Conventional (fixed) droop control

In conventional droop control method, a control loop is used to linearly reduce the output voltage reference when the output power increases. This is illustrated in Figure 2. 13. The output power of power electronic converter is inversely proportional to the droop coefficient [10].

In this droop control method, higher droop resistance results in increased accuracy in power sharing, but also an increased bus voltage deviation. On the other hand, smaller droop resistance result in reduced voltage deviations, but inaccurate power sharing. Therefore, in the conventional droop control approach, tradeoffs between power sharing between DGs and bus voltage stability have to be made. Furthermore, in conventional droop control, circulating current issues may arise due to the mismatch in converter output voltages.

B. Nonlinear droop control.

In an effort to improve both, power sharing and bus voltage stability, use of nonlinear droop control have been discussed in the literature [113-114]. Example characteristics curve of a nonlinear droop control is shown in Figure 2. 14. At low load conditions, as far as power losses and voltage regulation considered, it is preferable to have low droop resistance. It results in superior voltage regulation and increased system efficiency. However, when the load currents are high, it is desirable to increase the droop resistance to improve the current sharing accuracy and thus, avoid the overload conditions. At the same time, higher droop resistance results in improved damping of the voltage oscillations. Since the increase of droop resistance compromises the voltage regulation, in order to have acceptable voltage regulation, droop characteristics are shifted up to compensate for the resulting voltage drop. As illustrated in Figure 2.14, in nonlinear droop control, droop resistance increases as the load current increases. Moreover, the intersection of the droop line and the voltage axis increases due to the fact that a voltage shifting (ΔV_1 & ΔV_2) is required as load power increases to achieve desirable voltage regulation [113].

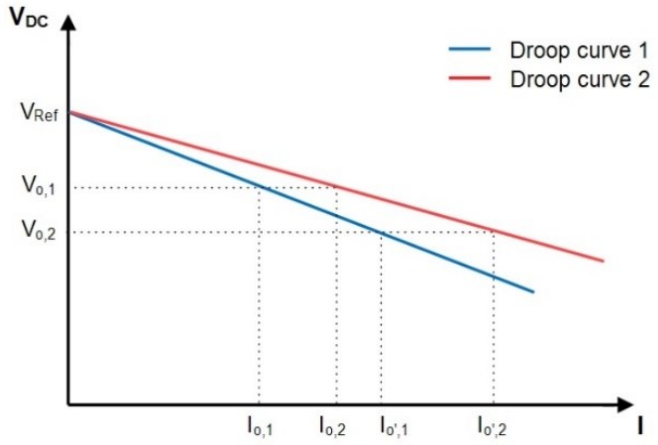

Figure 2. 13 Conventional droop control characteristic curve

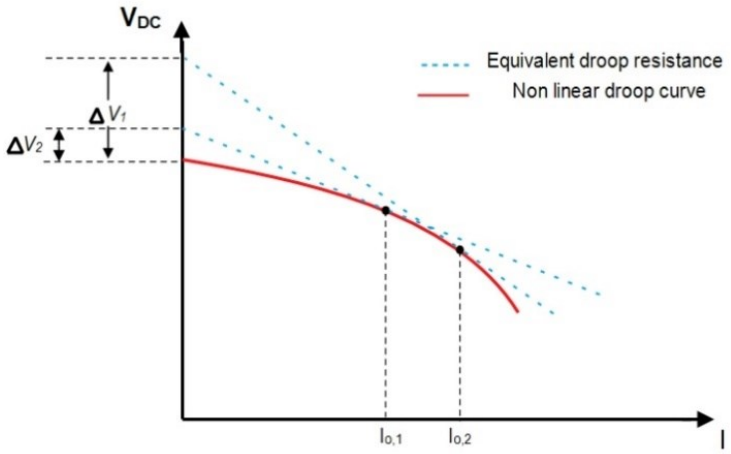

Figure 2. 14 Non-linear droop control characteristic curve

C. Adaptive droop control

Adaptive droop control methods have been proposed to adjust droop resistance to satisfy both power sharing and voltage stability requirements. In this approach, control parameters will self-adapt to provide optimal performance [111]. Several other adaptive droop control schemes such as fuzzy based adaptive droop control [115], consensus algorithm based adaptive droop control [116], impedance based adaptive droop control [117] have been proposed in the literature.

2. DC bus signaling based (DBS) control

In a DCMG, various DGs, ESSs and loads connected in parallel experience the same DC bus voltage, with cable resistance ignored. Thus, by detecting the DC bus voltage, the operating status of each converter can be determined [118,119]. The DBS control utilizes DC cables as the communication medium.

In DBS control, the range of operating voltages of the DCMG is divided into a number of sections, with operation mode defined for each section. With pre-specified control strategy rules for each operation mode, DBS control can achieve adaptive decentralized control of each parallel connected converter [118]. Figure 2. 15 shows an example DBS control scheme where four operating modes are defined [118]. In this control technique, DC bus voltage ranges are separately defined for each mode of operation as shown in Figure 2.15. For example, when DC bus voltage is between $V_{o,3}$ and $V_{o,4}$, DC microgrid operates in Mode II and controllers/control actions defined for the Mode II will take part in bus voltage control.

In general DBS control has the advantages of low cost, simpler control and no need for a communication link. However, DBS control is only suitable for a network with a limited number of DGs, ESSs and loads.

2.5.5. DC microgrid experimental setups worldwide

The research work on microgrids is based on testbeds and simulation studies. Testbeds, in particular, are instrumental in identifying practical issues associated and bring these technologies a step closer to a viable power system solution. Although the existence of DCMG experimental setups is still limited, DCMGs are gaining increasing research attention as a future power system.

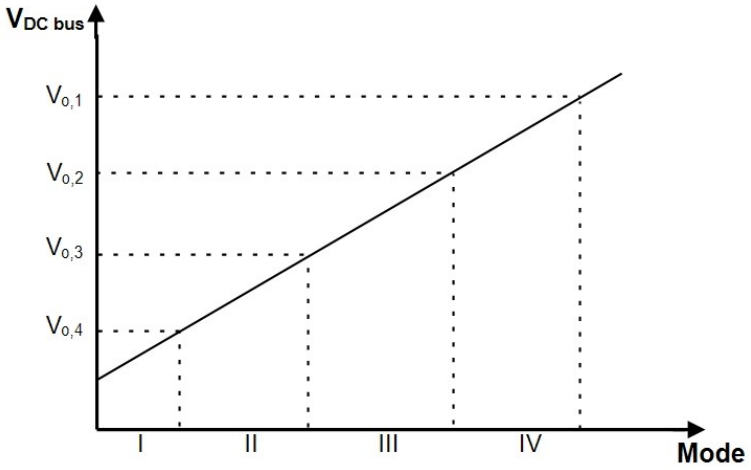

Figure 2. 15 DBS control with four operating modes for a DCMG system

Traditional DC distribution networks in the fields of telecommunication, traction and vehicular systems can be classified under the same DCMG framework. Developed standards, practical experience, and trends in these fields exert an important influence on the development of DC distribution networks. However, most of these networks are used for point to point applications. In contrast, DCMGs have a complex architecture and impose several control challenges as discussed in Section 2.5.2.

Several DCMGs have been implemented at laboratory level as test prototypes, or to supply power to commercial and residential loads. Table 2.1 provides an overview of the state of the art DCMG networks typically used as a test system or for a wide range of applications including residential, commercial, EV charging and electrifying rural areas.

Table 2. 1 DC microgrid experimental setups worldwide and their characteristic features

Project name	**Bus voltage/ capacity**	**Architecture**	**Loads/**	**DGs renewable**	**DGs non-renewable**	**Energy storage**	**Control architecture**
Sandia national lab test bed , Florida	400VDC/ 16kW	Radial	Residential	PV, Fuel cell	Diesel	Battery	Hierarchical
UT Arlington test bed, Texas	24VDC/ 10kW	Radial	Residential	PV, Wind, Fuel cell	Diesel, Gas	Battery	Decentralized
University of Miami test bed, Florida	N/A/ 10kW	Radial	Residential	PV, Fuel cell	-	Battery	Decentralized
FTU hybrid MG test bed, Florida.	300VDC/ 10kW	Radial	Residential	PV, Wind, Fuel cell	-	Flywheel	Centralized/ Multi agent
Bosch Honda facility test bed, California	380VDC/250kW	Radial	Commercial	PV	-	Battery, supercapacitor	Centralized
Burlington DCMG, Ontario, Canada	760/380VDC/ 160kW	Ring, Bipolar	Commercial/EV charging	PV	Diesel, Gas	Battery	N/A
Coconut island DCMG, Hawaai	N/A	Radial	Commercial/ Residential/ EV charging	PV, Wind, Fuel cell	Diesel	Battery	N/A
Kaucha ranch power park, Hawaii	48VDC/ 30kW	Radial	Residential	PV, Wind, Fuel cell	-	Battery	Centralized
Intelligent DCMG living lab, Aalborg university, Denmark	380/48/24/12VDC/ N/A	Radial	Residential	PV, Wind, Fuel cell	-	Battery	Centralized
CESI RICERCA DER test bed, Italy.	400VDC/ N/A	Radial	Residential	PV, solar thermal, Wind, CHP	Diesel	Battery	Centralized
University of Nottingham Test bed.	650VDC / N/A	Radial	Residential	Wind	-	Battery	Decentralized
University of Seville	48VDC	Mesh	Residential/ EV charging	PV, Fuel cell	-	Battery	Centralized
Nushima island DCMG	360VDC	Radial	Residential	PV, Wind	-	Battery	Centralized
Xiamen university test bed, China	240/380VDC/ 160kW	Radial	Residential/ Data center/ EV charging	PV	-	Battery	Centralized/ Decentralized
Hokkaido DCMG test bed, Japan.	380VDC	Radial	Commercial	PV	-	Battery	Centralized
Kalkeri Sangeet vidyalaya, India	240VDC, 15kW	Radial	Commercial	PV	-	Battery	Centralized

2.5.6. Standardization aspects of DC microgrids

Apart from the protection issues discussed above, lack of standardization is an impediment against widespread adoption of DCMGs. Standardization is essential to ensure safety, improve the reliability and reduce the costs of DCMG systems. Under this section existing standards and those under development related to DC networks are discussed and reviewed.

IEEE 964 standard provides the recommended practice for DC auxiliary power systems for generating stations and part of the content of this standard can be applied to DCMGs [120]. It provides guidelines for the design and operation of lead-acid batteries in DC systems including number of batteries, battery capacity, duty cycles, voltage levels and battery charger. Typical DC distribution system architecture is shown in this standard and briefly discusses the effect of grounding on the operation of DC auxiliary systems [120].

The IEEE 1547.4 standard provides the specifications for integration of microgrids with electric power systems [121]. This standard is designed for AC systems. However some sections are applicable to DCMG systems. IEEE 1547.4 standard is regarded as the fundamental standard guideline for microgrids, and focuses on requirements relevant to design, operation and integration of microgrid systems to the utility grid. This standard also discusses the modes of operation of the microgrid systems and explains the planning and engineering of microgrid systems [121].

IEEE DC@Home committee is established for developing standards and defining the roadmap for research and commercialization of DCMGs [122]. More specifically, primary objectives of this committee include;

i. Determine the standards that should be followed.
ii. Identify research required to improve and develop DCMGs.
iii. Make preliminary recommendations on how DC should be supplied and evaluate losses on supply to DC homes.

IEEE P2030.10, standard for DCMGs for Rural and remote electricity access applications, is a new IEEE standard project sponsored by IEEE PES/T&D. This standard covers the design, operations and maintenance of a DCMGs for rural and remote applications. The standard further provides requirements for providing LVDC

and LVAC power to off grid loads. It is intended to provide the framework to allow the deployment of DGs and ESSs [123].

National electric code (NEC) consists of articles and clauses that regulate the utilization and installation of DC technologies [124]. In 2017, new articles 706, 710 and 712 were added, covering energy storage systems, standalone systems and DCMGs respectively. Outlines of the articles include;

i. Article 250; guidelines and limitations regarding DC network grounding and bonding.
ii. Article 625; guidelines for charging systems of EVs and different charging levels.
iii. Article 690; guidelines for photovoltaic systems with standalone or interactive, with or without ESSs. Circuit schematics for different configurations.
iv. Article 706; provides requirements covering ESSs that can be standalone or interactive with other power sources and that actively supply DC loads.
v. Article 710; requirements of power sources operating in standalone mode.
vi. Article 712; covers DCMGs that are powered by at least two interconnected DC sources. The article provides specifications regarding system grounding, including ground fault detection equipment, overcurrent protection, interrupting and short circuit current ratings, identification of circuit conductors and DC source disconnecting mean.

International standards and specifications that are prepared by several IEC committees and sub committees, which are related to LVDC are available and summarized in [125]. These standards cover range of different aspects of DC networks including individual components, tests and ratings. IEC standardization management board (SMB) agreed to setup a system evaluation group (SEG 4), to evaluate the status of standardization in the field of LVDC applications and products. The SEG 4 will identify new areas of standardization to be undertaken by IEC and will evaluate the use of LVDC in developed and developing economies [126].

Emerge alliance is an open industry association leading the rapid adoption of safe DC power distribution in commercial buildings through the development of standards. This standard also defines control systems necessary to monitor and

control devices and power sources [127]. Emerge Alliance data/ telecom center standard is intended to address number of growing challenges in designing, building and operating data/telecom centers in commercial buildings. This standard defines 380 VDC infrastructures that interconnect sources of power to devices in the data/telecom centers, which draw the power [128].

The efforts by International Telecom Union (ITU) and the European Telecom Standard Institute (ETSI) to standardize and promote the use of DC distribution systems for Data/telecom applications are summarized in [129]. Outline of the currently issued DC power standards by ITU and ETSI are:

i. ETSI EN 300 132-3-0; power interface standard.
ii. ETSI EN 301 605; earthing and bonding of 400VDC data and telecom equipment.
iii. ITU-T L.1200 (2012-05); DC power feeding interface up to 400V at the input to telecommunication and ICT equipment.
iv. ITU-T L.1201 (2014-03); Architecture of power feeding systems up to 400VDC.

Table 2.2 summarizes the standards/standardization efforts mentioned in this Section [120-129].

Table 2. 2 General description and scope/ primary goals of standards/standardization efforts for DCMGs

Standard	General description	Scope/ primary goals
IEEE 964	Standard for design of the DC auxiliary power systems in generating stations.	• Components of the DC system addressed by this recommended practice include lead acid batteries, static battery chargers and distribution equipment. • Guidance for selecting the equipment ratings, interconnections, instrumentation, control and protection is provided.
IEEE 1547.4	Standard for integration of microgrids with electric power systems.	• Designed for AC microgrid systems, but can be used a reference for DC systems. • Provides requirements relevant to performance, operation, testing, safety and maintenance of interconnections to the power system.
IEEE DC@Home	Established for developing standards and defining the roadmap for research and commercialization of DCMGs	• To determine the standards that should be followed • Identify research required to improve and develop DCMGs. • To make preliminary recommendations on how DC should be supplied and evaluate losses on supply to DC homes.
IEEE P2030.10	Standard for DCMGs for Rural and remote electricity access applications	• Covers the design, operations and maintenance of a DCMGs for rural and remote applications.

NEC standards	Articles and clauses that regulates the utilizing and installation of DC technologies	• Guidelines and limitations regarding DC network grounding and bonding. • Requirements covering ESSs that can be standalone or interactive with other power sources and that actively supply DC loads. • Requirements of power sources operating in standalone mode.
IEC standards	Several standards, technical reports and technical specifications for components and systems central to LVDC available currently with more being developed.	• Cover range of different aspects DC networks including individual components to complete systems, tests and ratings. • IEC SEG4 will identify new areas of standardization to be undertaken by IEC and will evaluate the usage of LVDC in developed and developing economies.
Emerge alliance DCMG standards	Standards for occupied spaces and data/telecom centers.	• Occupied space standard define DCMG power distribution infrastructure layer that interconnects sources of power to devices in the space which draw the power. • Data/telecom center standard is intended to address number of growing challenges in designing building and operating data and/or telecom centers in commercial buildings.
ITU and ETSI standards	ITU and ETSI standards to promote the use of DC distribution systems for Data/telecom applications	• Standards cover the aspects such as power interfaces, earthing, network architectures and methodologies for evaluating the performance of networks.

2.6.Concluding remarks

Fast current rise caused by capacitor discharge imposes strict time limits for fault interruption in DC networks. In this regard, the speed of fault detection and response time of fault interruption equipment are important aspects to be considered. Furthermore, the natural absence of zero crossing requires the DC switchgear to employ additional means to force current zero compared to conventional AC switchgear.

Due to the Absence of phasor and frequency information, conventional directional elements for fault localization in AC networks cannot be employed. Advanced machine learning and signal processing based techniques were identified as a reliable solution for detection and localization of faults in DC networks with its fast, accurate and intelligent detection capabilities.

Although SSCB technologies offer a promising solution with their fast fault interruption capability, high on-state losses and high costs associated impose

limitations on the widespread adoption of these technologies. However, the next generation SiC and GaN devices may improve these SSCB technologies with their low conduction losses and high junction temperatures, which significantly reduce the cooling requirements.

A protection coordination scheme to minimize outages with the minimum opening approach is an essential requirement for the reliable operation of DC microgrids. DC breakers working in coordination with DC network converters to minimize damage to the network can prevent damages to the network while minimizing interruptions. Further research in these areas are required.

3. DC MICROGRID MODELLING AND CONTROL

A discussion on the modeling and validation of the notional DCMG test system used in this study is presented in this chapter.

The schematic diagram of the notional DC microgrid model in PSCAD/EMTDC is shown in Figure 3.1. Control objectives of each individual component can be summarized as follows:

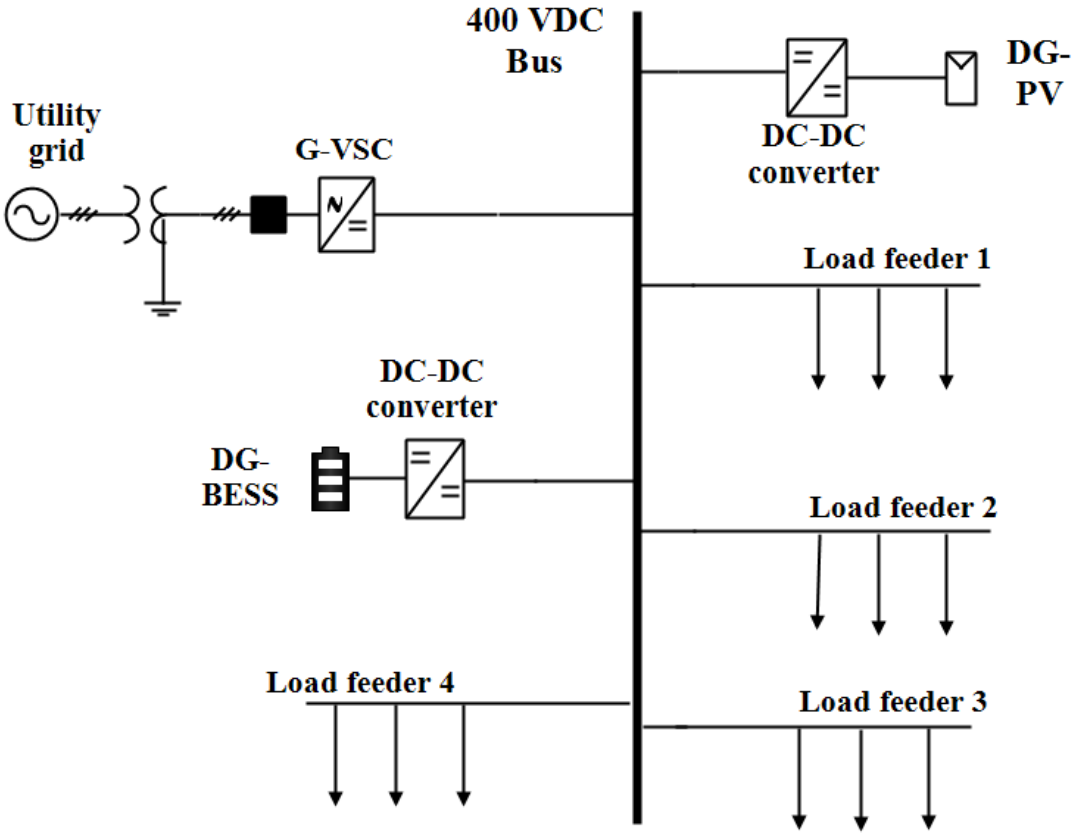

Figure 3. 1 Notional DC microgrid model developed in PSCAD/EMTDC

• **Two-level grid-connected voltage source converter (G-VSC)** controls the DC bus voltage, V_{DC} at the nominal value and accommodates power fluctuations.

• **Energy Storage System (ESS)** connected to the DC bus by a DC-DC bidirectional converter. The ESS functions as the bus voltage regulator during the islanded operation where G-VSC control action is absent, or whenever the G-VSC loses its ability to regulate V_{DC}.

• **Solar PV plant** connected to the DC bus by a unidirectional boost converter. It usually operates at the maximum power point tracking (MPPT) mode. Also, it operates in voltage control mode to curtail the generation in an islanded system.

• **DC loads** modeled as linear loads and fixed power loads to represent variable loading conditions. A suitable load shedding scheme is adopted for load management.

As discussed in Section 2.5.2 the main control objectives of a DCMG include regulating DC bus voltage with minimal fluctuations and efficient power sharing among AC utility grid, RESs and loads connected to the network. ESSs increase operational reliability and reduce the need for load shedding during islanded operation. Battery energy management system (BEMS) acts as supervisory control, which regulates voltage while managing battery energy level through the state of charge (SOC) measurement. Load shedding/generation curtailment schemes take part in regulating V_{DC} during islanded operation and faults.

DCMG system was modeled in PSCAD/EMTDC, in accordance with control requirements discussed in Section 2.5.2. Table 3.1 lists the characteristic data of the DCMG model. The DC cables selected: 0.6/1.0 kV cables with line impedance of 0.427+0.125j Ω/km. The loads are modeled as distributed loads along the load feeder. The control strategy employed in designing the DCMG model is discussed in Section 3.1.

Table 3. 1 Characteristic data for the developed DCMG model in PSCAD/EMTDC

Point of common coupling(PCC) voltage L-L	200 V
DC nominal bus voltage	400 VDC
G-VSC nominal power	100 kW
Battery nominal power	50 kWh
Battery nominal voltage	240 V
Battery capacity	200 Ah
PV plant nominal power	60 kW
PV plant short circuit current	450 A
PV plant open circuit voltage	180 V
Load feeder 1(cable length: 100m)- ΔV_{La1} = 0.2 p.u; ΔV_{Lb} =0.1 p.u, t_{K1}= 1 s	15 kW
Load feeder 2(cable length: 50m)- ΔV_{La2} = 0.2 p.u; ΔV_{Lb} =0.1 p.u, t_{K2}= 1 s	25 kW
Load feeder 3(cable length:50m)- ΔV_{La3} = 0.2 p.u; ΔV_{Lb} =0.1 p.u, t_{K3}= 2 s	15 kW
Load feeder 4- critical loads (cable length: 100m)- ΔV_{La4} =-; ΔV_{Lb} =-, t_{K4}= -	15 kW

3.1. DC Microgrid control strategy

This Section details the control strategy employed in the development of DCMG model for the protection study. Distributed control topology with DC bus voltage signaling is employed in this model for DG control and coordination.

3.1.1. G-VSC control

The main control objective of the G-VSC is to regulate the DC bus voltage of the DCMG. Voltage based control method implemented in ***dq*** domain was adopted when designing the controllers for the VSC (see Figure 3.2). Variables V_{abc} and I_{abc} are the measured grid side voltage and current, i_d and i_q represent the ***d*** and ***q*** axis components of grid-side current, while V_d and V_q represent the ***d*** and ***q*** axis components of grid voltage. The control scheme determines the phase angle and G-VSC terminal voltage to generate the required input current. The reference value for active current component is generated by the outer voltage control loop, which regulates the DC bus voltage, V_{DC} [130]. Variables, V_{dI}^{ref} and V_{qI}^{ref} represent the ***d*** axis and ***q*** axis reference voltages calculated by the VSC control scheme.

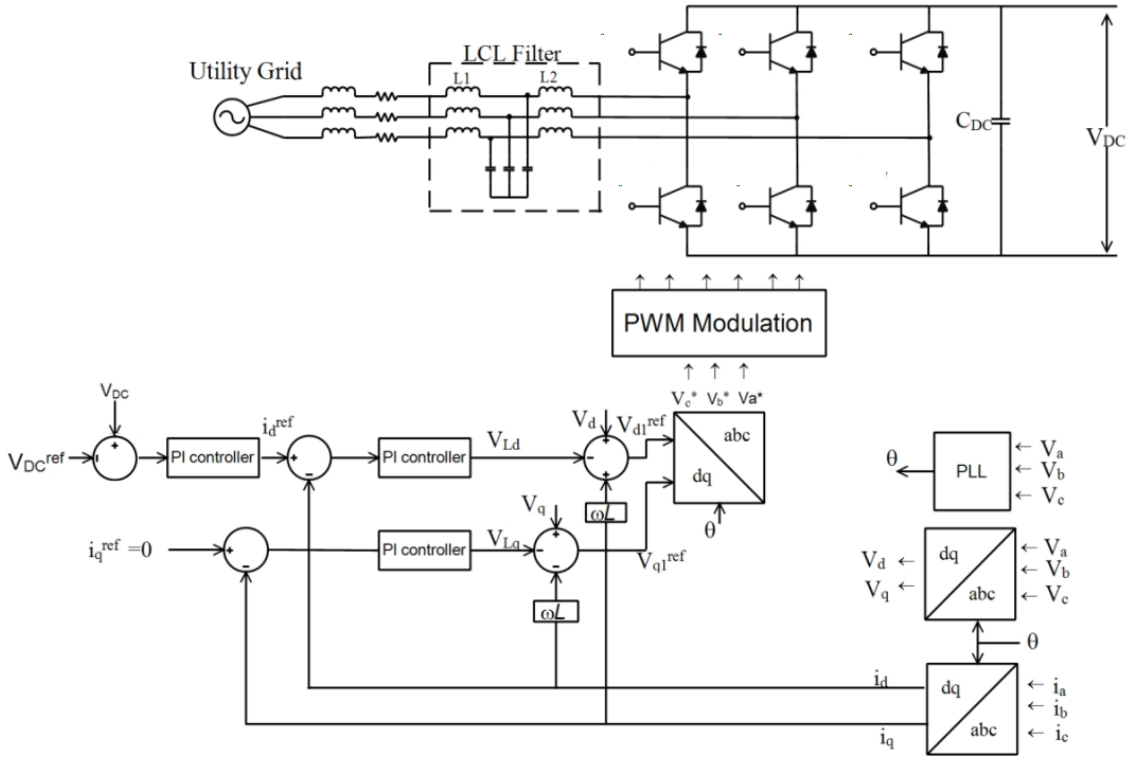

Figure 3. 2 Schematic of the G-VSC control

3.1.2. Solar PV plant control

The solar PV plant is required to operate at maximum power point tracking (MPPT) voltage to harness the maximum power as shown in Figure 3.3. If the generation is required to be curtailed, solar PV plant starts to operate in voltage control mode. The literature discusses several MPPT algorithms [131]. Most commonly used MPPT algorithm, perturb and observe (P&O), was employed in this study.

In the DC/DC bidirectional converter, dual control loop with outer voltage and inner current control is adopted to achieve an improved control performance. The outer voltage loop takes converter input voltage V_{pv} of the PV system as controlled variable. Variable, I_L is the converter inductor current. Inductor current reference, I^{ref} is the output of the PI compensator of the voltage control loop. Required MPP duty ratio is generated by the inner current control loop. In MPPT mode, output voltage of the DC-DC converter V_H, is determined by the duty ratio of the converter required to maintain V_{MPP} at the DC-DC converter input. However, since the DC-DC converter is interfaced to the DC bus, V_H takes the same voltage as V_{DC}.

Under islanded operation, ESS is required act as the primary DC bus voltage controller. However, when the ESS is not capable of regulating the DC bus voltage (due to battery SOC level reaching its upper or lower limits, or required current exceeds battery current limits), it is required to curtail the solar PV generation or shed loads. This is shown in Figure 3. 3. Outer voltage control loop regulates the output voltage of the DC-DC converter, V_H to follow the reference voltage, V_H^{ref}.

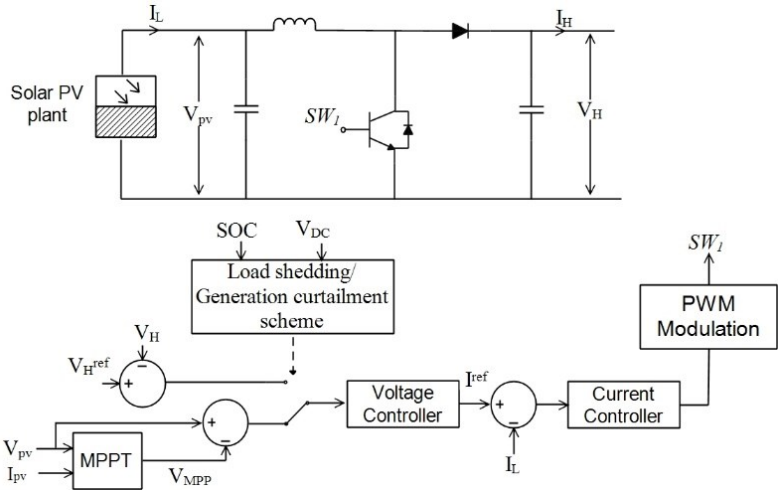

Figure 3. 3 Solar PV plant control scheme

3.1.3. ESS control

For a DCMG system, it is important to control the V_{DC} within acceptable limits. Since DGs such as solar PV are intermittent in nature, and loads operate according to its own profile, battery energy storages are required to cater to any power mismatch arising. Compared to AC networks, in DC networks response to variations in loads and supply power should be fast, in order to minimize fluctuations in bus voltage, and maintain the bus voltage stability. Battery storages have very quick response times; hence, can be used to compensate for any power mismatches. As the ESS is required to operate under different modes of operation Battery energy management system (BEMS) is crucial for effective and reliable operation of ESS.

For controlled power transfer, a bidirectional DC/DC converter is used in this study for charge/discharge operation of ESS and is shown in Figure 3.4. The PI compensator of the outer voltage control loop processes the V_{DC} error compared with the reference voltage, V_{ESS}^{ref} determined by the BEMS. Consequently, converter terminal voltage, V_{ESS} is determined by the BEMS. However since the battery storage is interfaced to the DC bus, V_{ESS} is equal to the V_{DC}. In the control scheme employed inner current control loop is adopted for battery current control. The BEMS determines the charge, discharge or idling operation of the ESS by selecting the maximum charging and discharging current limits (I_{max_chg} and I_{max_dis}) of the converter, and is further discussed in Section 3. 2.

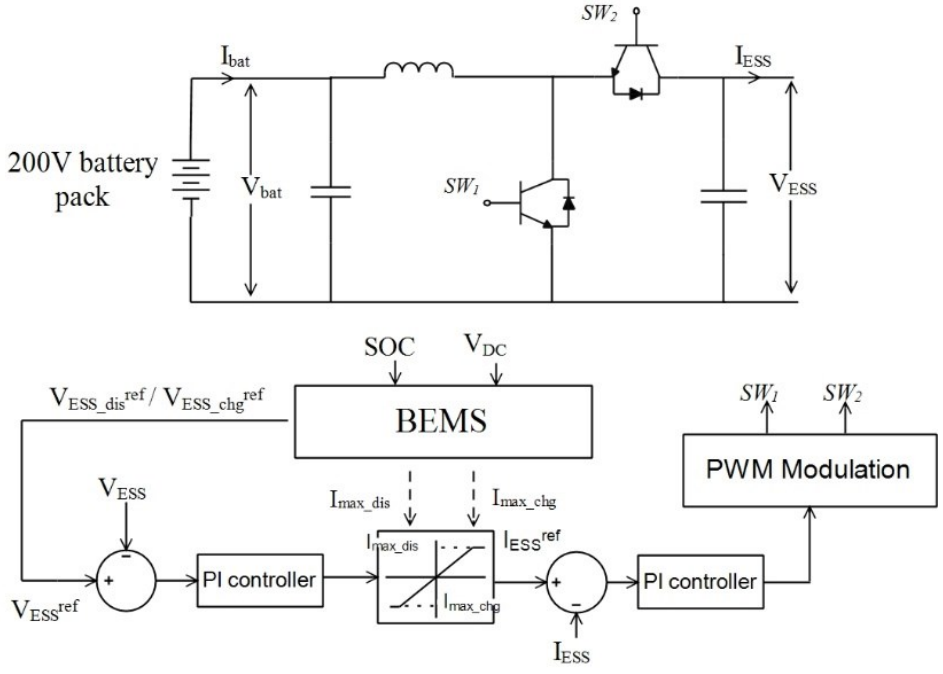

Figure 3. 4 ESS control block diagram

3.2. Battery Energy management system

Figure 3.5 shows the battery energy management scheme adopted to maintain the DC bus voltage, while ensuring efficient operation of battery storage. Over-charging/discharging degrades the battery performance and reduces battery lifetime. Hence, an upper and lower SOC limits are defined for a battery system. Operation SOC range depends on the type and ratings of the battery employed. In this study upper SOC limit, $\boldsymbol{SOC_{max}}$ = 90% and lower SOC limit, $\boldsymbol{SOC_{min}}$ = 40% is selected.

Battery energy management system (BEMS) is required to limit unnecessary charge/ discharge cycles. Hence, interfacing converter is set to enable charge/discharge only when the $\boldsymbol{V_{DC}}$ variation from the nominal exceeds a preset limit. This is achieved through a reference charging voltage $\boldsymbol{V_{ESS\_chg}^{ref}}$, and reference discharging voltage $\boldsymbol{V_{ESS\_dis}^{ref}}$. Hence, the system operating mode can be detected by all network components via common DC bus voltage. In addition, to prevent any damages to equipment and prolong battery life, maximum charging current, $\boldsymbol{I_{max\_chg}}$ and discharging current, $\boldsymbol{I_{max\_dis}}$ is set. The SOC and $\boldsymbol{V_{DC}}$ are required as inputs to BEMS to carry out its control functions. The values $\boldsymbol{I_{max\_dis}}$ and $\boldsymbol{I_{max\_chg}}$ determine whether the EES charge/discharge or in idling operation; hence these values are used as input for the control logic to generate switching signal for the DC/DC converter. To achieve DC bus voltage control, BEMS set the voltage references $\boldsymbol{V_{ESS\_chg}^{ref}}$ and $\boldsymbol{V_{ESS\_dis}^{ref}}$ according to four modes of operation as discussed below. Based on the associated unit for $\boldsymbol{V_{DC}}$ control and voltage references, five-level voltage control hierarchy is employed for the DCMG, as shown in Figure 3. 6.

3.6.1. Operating mode 1

This mode corresponds to the grid-connected mode where G-VSC caters to the power variations caused by varying generation and loads to regulate bus voltage at nominal, $\boldsymbol{V_{DC}^{nominal}}$. ESS operates in idling mode when G-VSC regulates the DC bus voltage and if G-VSC cannot cater to the temporary power variations on its own, ESS accommodates it. Therefore, in idling operation, both $\boldsymbol{I_{max\_chg}}$ and $\boldsymbol{I_{max\_dis}}$ is set to zero to block the charging and discharging operation of the ESS. This operation corresponds to level 3 voltage control shown in Figure 3. 6. If there is a temporary voltage drop due to the inability of G-VSC to regulate the bus voltage, ESS operates in discharge mode with $\boldsymbol{V_{ESS\_dis}^{ref}}$ as the reference voltage. $\boldsymbol{I_{max\_chg}}$ is set to zero by

BEMS so that ESS can only operate in discharge mode (Level 2 voltage control in Figure 3. 6). Similarly, if there is a temporary voltage rise BEMS will set the I_{max_dis} to zero so that ESS can only operate in charging mode. ESS reference voltage will be set to $V_{ESS\_chg}^{ref}$ (Level 4 voltage control in Figure 3.6).

3.6.2. Operating mode 2

This mode corresponds to events in the DCMG system where G-VSC cannot regulate V_{DC} . Hence, ESS takes part in regulating V_{DC}. In this mode DCMG operates in either level 4 or level 5 voltage control (see Figure 3.6). When ESS operates in discharge mode with a reference voltage of $V_{ESS\_dis}^{ref}$, I_{max_chg} is set to zero so that ESS can only operate in discharge mode. However, prolonged operation in this mode can lead to draining out of the battery energy. Therefore, critical SOC level, $SOC_{critical}$ (50%) is defined, below which, reference voltage $V_{ESS\_dis}^{ref}$ takes a lower value (0.8 p.u as shown in Figure 3. 6). This triggers the load shedding through bus voltage signaling (level 5 voltage control). This is further discussed in Section 3.3.

3.6.3. Operating mode 3

In the islanded mode ESS acts as the primary V_{DC} regulator. ESS operates in both charging and discharging modes with voltage reference $V_{ESS\_chg}^{ref}$ and $V_{ESS\_dis}^{ref}$ respectively. When $P_{pv} > P_{load}$, ESS is not allowed to discharge ($I_{max\_dis} = 0$) and $V_{ESS}^{ref} = V_{ESS\_chg}^{ref}$ is set allowing charging operation (Level 4 voltage control). When $P_{pv} < P_{load}$ ESS is not allowed to charge ($I_{max\_chg} = 0$) and $V_{ESS}^{ref} = V_{ESS\_dis}^{ref}$ is set allowing discharging operation (level 2 voltage control).

3.2.4. Operating mode 4

The prolonged islanded operation will cause the battery to fully charge or drain out. If SOC level reaches SOC_{max} (= 90%) due to continued charging operation, ESS can no longer regulate bus voltage as charging is halted ($I_{max\_chg} = 0$). Hence generation curtailment has to be carried out (level 5 voltage control). Continued operation in discharging mode will cause the SOC level to reach $SOC_{critical}$ (50%), which will require load shedding to guarantee the supply to the critical loads (level 1 voltage control). This load shedding scheme is discussed in Section 3. 3. Faults during islanded mode may also result in ESS not being able to regulate V_{DC} and load shedding scheme have to take part in bus voltage regulation.

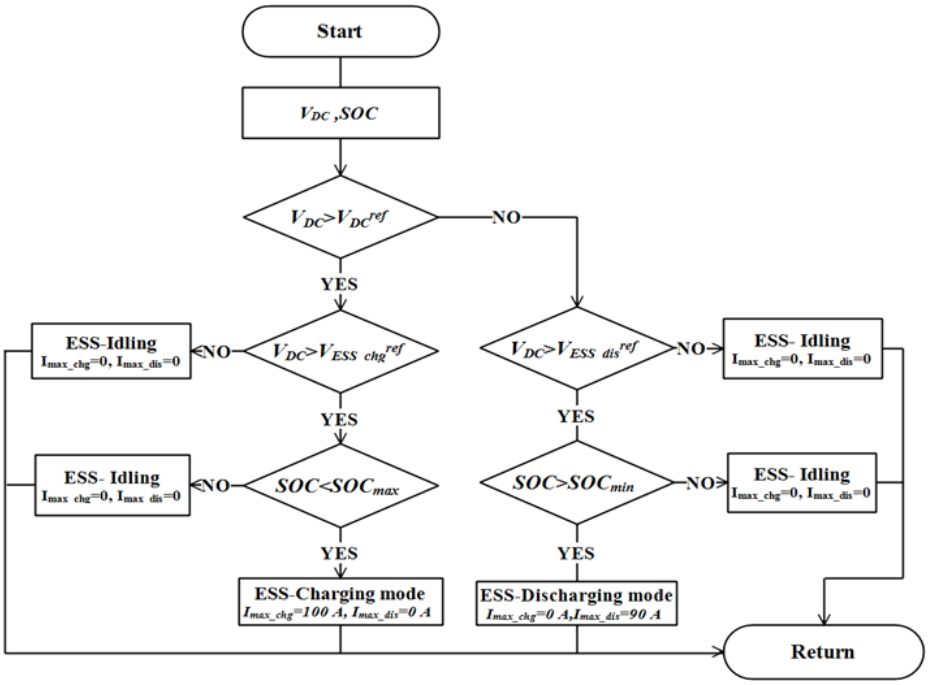

Figure 3. 5 Proposed BEMS control algorithm for the DCMG model

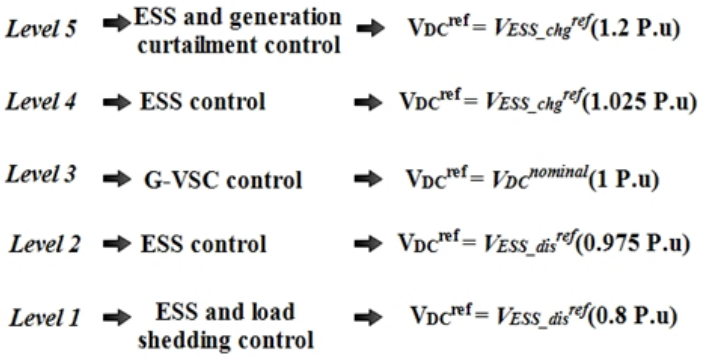

Figure 3. 6 Five-level voltage control hierarchy.

3.3. Load shedding and generation curtailment

Load management, which involves load shedding based on predefined load priority levels, is necessary during islanded and abnormal conditions. In this paper load shedding strategy based on two voltage deviation settings is proposed. The DC voltage deviation, ΔV_{DC} is defined as (3.1);

$$\Delta V_{DC} = V_{dc}^{nominal} - V_{dc} \qquad (3.1)$$

Two voltage deviation settings are defined for each load feeder, and the loads are prioritized to ensure that those with highest priority level trip last or do not trip at all. First voltage deviation setting, ΔV_{LaK} corresponds to the immediate trip of the

relevant load (K=1,…., n for loads 1,…, n respectively). The second voltage deviation setting, ΔV_{Lb} is common for all loads and will trip the loads if the ΔV_{DC} remains above this value for a time duration t_K. Loads with lowest priority level have the lowest ΔV_{LaK} and shortest t_K duration and vice versa. The proposed load shedding algorithm for load feeder 1 is shown in Figure 3. 7.

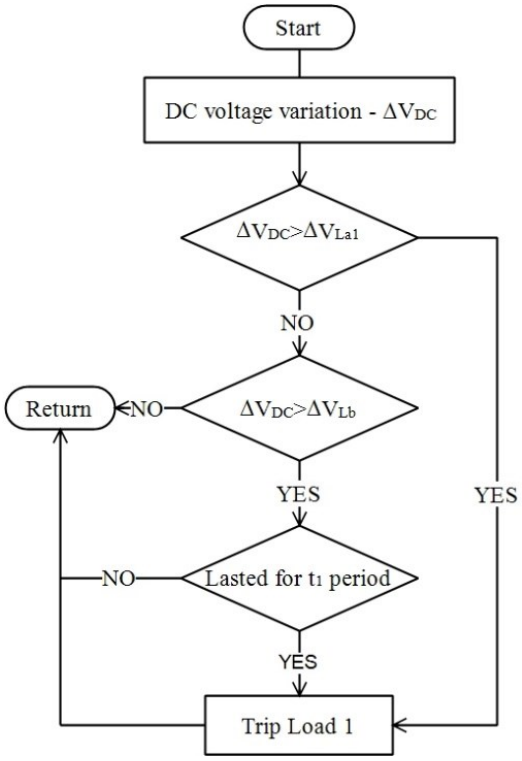

Figure 3. 7 Proposed load shedding scheme for DCMG load feeders

3.4. DC Microgrid model validation

DCMG system simulation studies were carried out using PSCAD/EMTDC, in accordance with four operating modes discussed. Accordingly, four cases were studied under each operating mode to evaluate the performance of the developed DCMG model.

Case 01:

Case 01 corresponds to the grid-connected operation (operating mode-1). The simulation results for operating events listed in Table 3.2 are shown in Figure 3.8. Initially, load feeders 1, 3 and 4 are switched in. As the system is grid-connected V_{DC} is regulated mainly by G-VSC at 400 VDC, and is shown in Figure 3.8 (a). The trend of G-VSC power, G-VSC DC side current, Solar PV power, ESS power and load

Power are shown in Figure 3.8 (b)-(f) respectively. The simulation results show that the G-VSC is capable of regulating the V_{DC} at 400V and ESS share part of temporary power fluctuations to regulate V_{DC}.

Table 3. 2 Operational events for case 01

Event	Operating condition	Time
1.	P_{pv} decrease	2.00 s
2.	Load feeder 2 switched in	3.00 s
3.	P_{pv} increase to nominal	4.00 s
4.	Load feeders1,2 and 3 switched out	5.00 s

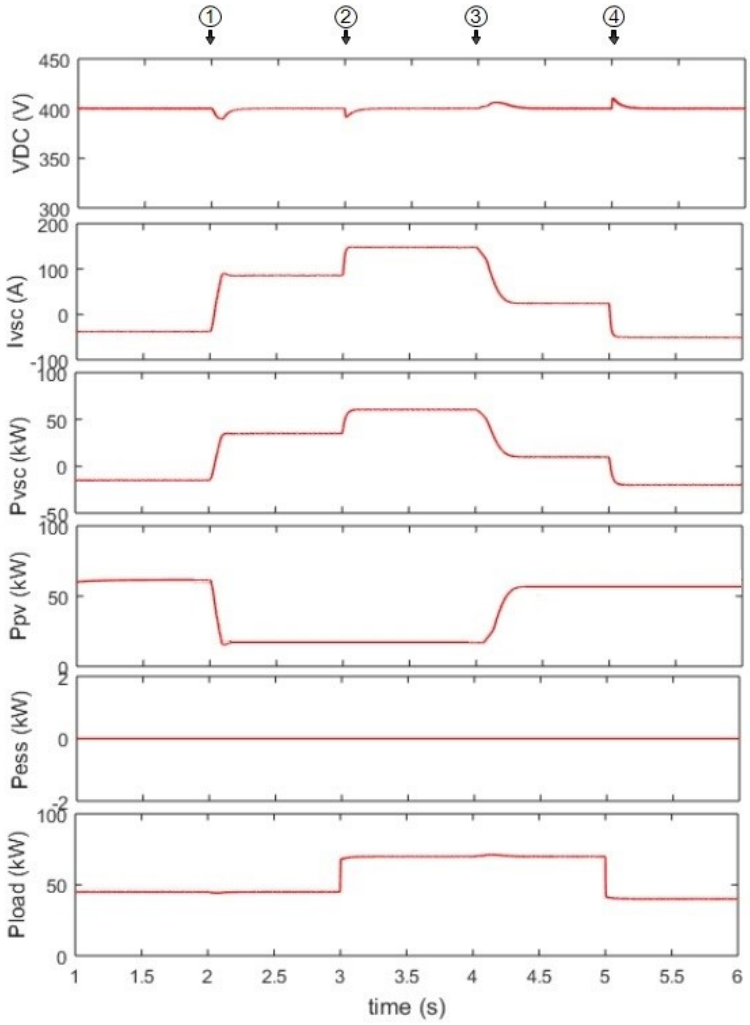

Figure 3. 8 Operation during grid-connected mode, (a) DC bus voltage, (b) G-VSC DC current, (c) G-VSC power, (d) solar PV power, (e) ESS power, (f) Load power

Case 02:

Simulations results for events (Table 3.3) corresponding to operating mode-2 are shown in Figure 3.9. In this case, it is assumed that all load feeders are switched-

in initially. The simulation results show that G-VSC and ESS maintain the V_{DC} at 0.975 p.u. during AC grid side fault. However, they lose controllability during the DC fault, and require the load shedding scheme to take part in maintaining bus voltage stability. As can be seen in Figure 3.9 (f), load feeders 1, 2 and 3 are shed following the DC fault.

Table 3. 3 Operational events for case 02

Event	Operating condition	Time
1.	Three phase AC short circuit fault of 500ms	2.00 s
2.	AC side Fault cleared	2.20 s
3.	Load feeders 1 and 3 (15kW+15kW) switched in.	3.00 s
4.	PV generation halted, G-VSC reaches power limit	4.00 s
5.	Load feeders 1 and 2(15kW+20kW) switched out, PV generation restart	5.00 s
6.	200ms DC side short circuit fault cause Both G-VSC and ESS to lose controllability.	5.50 s
7.	DC fault cleared	5.70 s

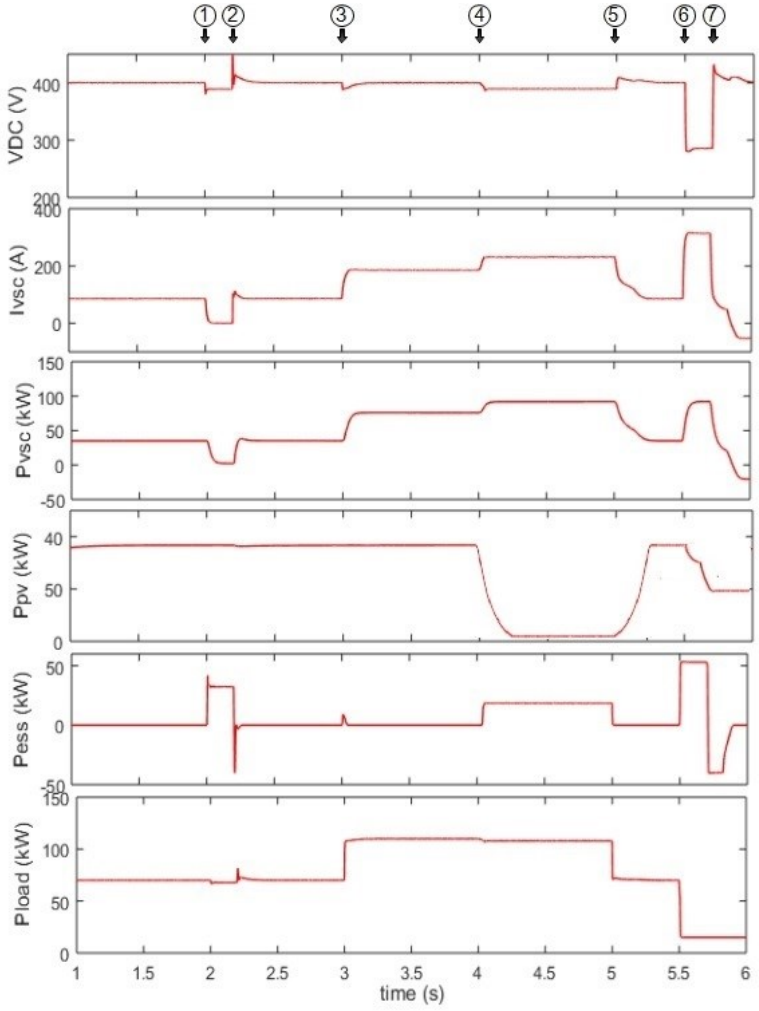

Figure 3. 9 Operation during grid-connected mode (case 2).(a) DC bus voltage, (b) G-VSC DC current, (c) G-VSC power, (d) solar PV power, (e) ESS power, (f) load power.

Case 03:

Simulation results for events (Table 3.4) in operating mode-3 are shown on Figure 3.10. It is assumed that initially load feeders 1, 3 and 4 are switched in. The initial SOC level is assumed at 60%. Here, V_{DC} is successfully regulated at 1.025 p.u and 0.975 p.u (see Figure 3.10 (a)), by ESS through charge and discharge operation as shown in Figure 3.10 (d).

Table 3. 4 Operational events for case 03

Event	Operating condition	Time
1.	AC grid disconnects	2.00 s
2.	Solar PV generation decrease	3.00 s
3.	Load 2 switch in	4.00 s
4.	Solar PV generation increase	5.00 s

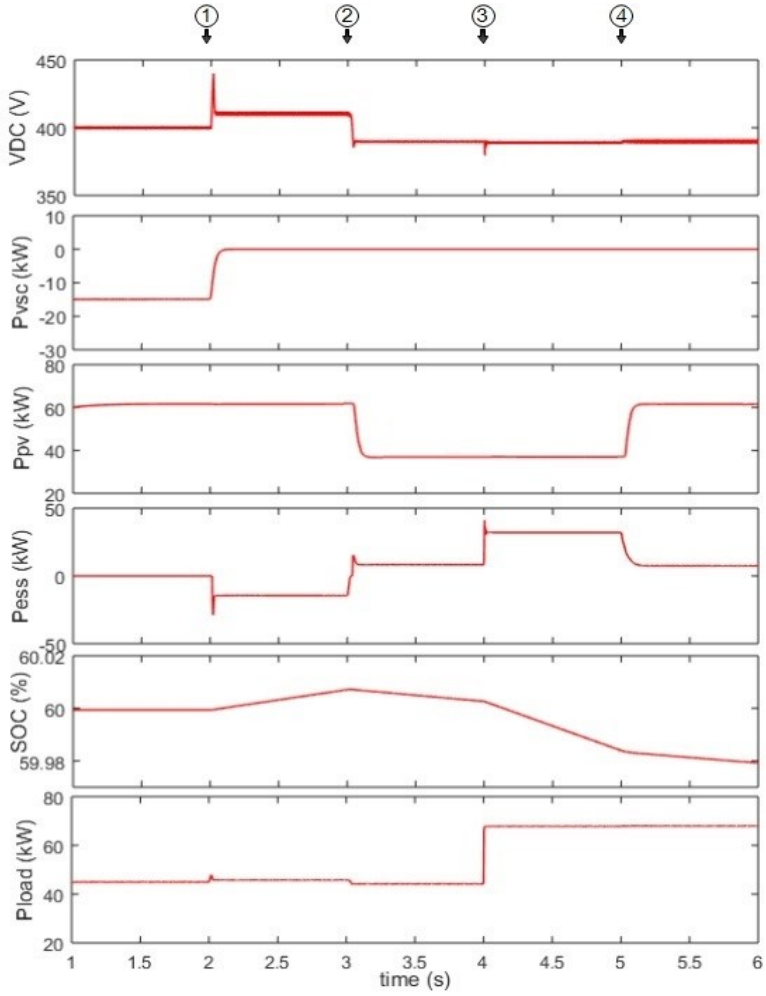

Figure 3. 10 Operation during islanded mode (case 3), (a) DC bus voltage, (b) G-VSC power, (c) solar PV power, (d) ESS power, (e) SOC level (f) load power.

Case 04:

The simulation of DCMG operation corresponding to events (see in Table 3.5) in operating mode-4 is shown in Figure 3.11. The initial SOC level is assumed closer to $SOC_{critical}$, 50%. It's also assumed solar PV plant generates low power level and load feeders 1, 2, 3 and 4 are switched in initially. As seen in Figure 3.11 (d) load shedding scheme take part in V_{DC} regulation, during DC fault (at t = 3.00 s) and when $SOC_{critical}$ is reached (at t = 4.30 s). V_{DC} is regulated successfully except during DC fault (at t = 3.00 s).

Table 3. 5 Operating events for case 04

Event	Operating condition	Time
1.	AC grid disconnects	2.00 s
2.	DC side short circuit fault of 200ms and ESS loses its controllability, Loads 1,2 and 3 are shed	3.00 s
3.	Fault cleared in 200ms	3.20 s
4.	Loads are restored in 200ms	3.40 s
5.	SOC level reach 50%, Loads 1,2 and 3 are shed	4.30 s

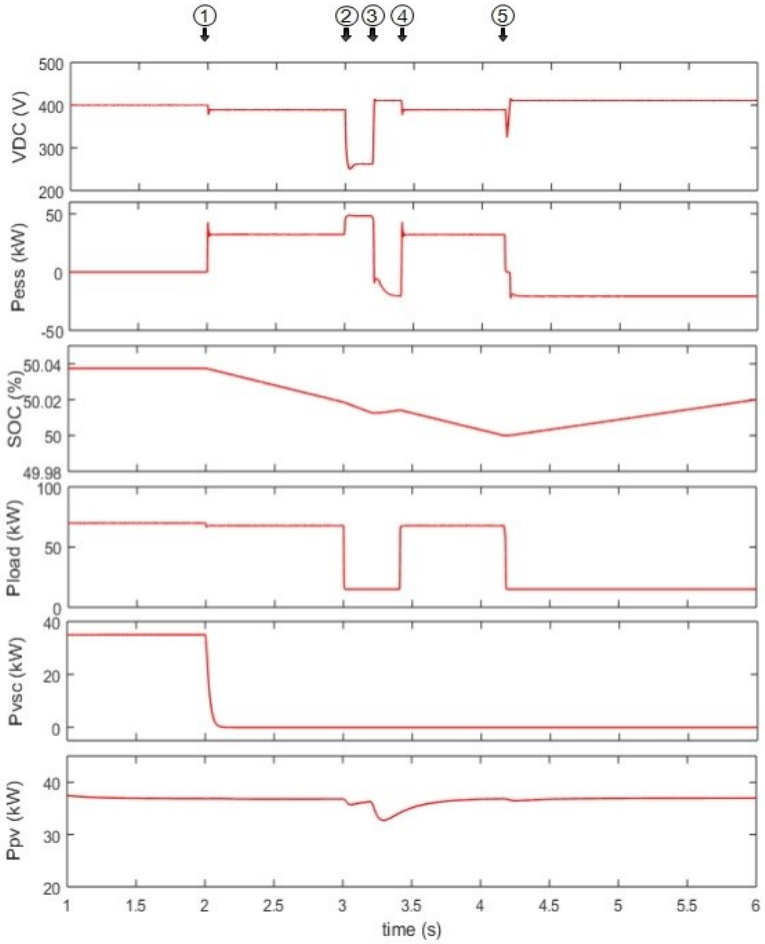

Figure 3. 11 Operation during islanded mode(case 4).(a) DC bus voltage, (b) ESS power, (c) SOC level, (d) load power,(e) VSC power (f) solar PV power.

4. DC MICROGRID FAULT RESPONSE ANALYSIS

For the protection of DCMGs, reliable detection of faults occurring in the network is important. The fault response of a network depends on fault type and location. Faults in a DCMG can occur in the DC bus, within converters, DG sources and load feeders. Often pole-pole faults are low impedance faults, while pole-ground faults can be either low impedance or high impedance faults [39, 132, 133].

Other key factors which influence the post fault behavior of the network are:

1) Interconnecting DGs and power electronic converters interfacing DGs.
2) Fault impedance.
3) Grounding configuration employed.
4) DC network architecture.

4.1. DCmicrogrid Transient behavior

Subsequent to a fault in a DC network, DC link capacitors discharge quickly causing transient capacitor discharge current and sudden fall of DC bus voltage. The capacitor discharge current transient magnitudes depend on total DC network capacitance and total fault loop impedance. Total DC network capacitance is the cumulative capacitance of power electronic converter and cables. Fault loop impedance is determined by fault impedance and fault location [39].

4.2. Power electronic converter behavior

As discussed above a fault in the DC network causes the DC side capacitors of the network converters to discharge rapidly. This Section discusses power electronic converter behavior subsequent to a fault in a DC network.

The desirable operation of an IGBT based converter is assured when antiparallel diodes across the IGBTs are reverse-biased by the DC link voltage of the converter capacitor. During a fault DC bus voltage, V_{dc}, falls due to the fast discharge of DC link capacitors. Following a fault, if V_{dc} drops below reverse bias voltage of the diodes, IGBT based power electronic converter starts to behave erratically. Current starts to freewheel through the diodes without control, and fault current will only be limited by fault current loop impedance [132, 133].

Generally, IGBT based converters embed self-protection schemes for overvoltage and overcurrent protection, and their protective actions should be taken into consideration when analyzing the power electronic converter fault response. Commonly used self-protection scheme, desaturation (DESAT) protection activates within 2 μs blocking OFF the operation of IGBTs [55, 56]. However, power electronic converters will continue to conduct fault current through freewheeling diodes of the converter, unless the network is equipped with fault detection and current interruption equipment [55, 56]. Freewheeling diodes are sensitive to over-currents; hence require suitable fault interruption scheme to interrupt the fault current in a timely manner [39, 132].

The fault response of a G-VSC and DC-DC converters are discussed under below Sections.

4.2.1. G-VSC post Fault behavior

VSC with a pole-pole fault in the DC side is shown in Figure 4.1(a). Low fault impedance, R_f, causes higher voltage drops; consequently, VSC loses its ability to control DC bus voltage.

Following a fault, if V_{dc} drops below $\mathbf{1.35\sqrt{3}}V_{an}$ (i.e. output voltage corresponding to a diode rectifier), where V_{an} is the line-phase voltage of the VSC input side, freewheeling diodes are forward biased and G-VSC is no longer PWM controlled. Hence, VSC starts to work irregularly, and the current through the VSC, I_{vsc} rises exceeding the converter nominal value. With IGBTs blocked by IGBT self-protection, there is no control action by VSC [132,133]. The fault current will continue to flow to the fault through antiparallel diodes. For low R_f values if V_{dc} does not dropped below $\mathbf{1.35\sqrt{3}}V_{an}$, freewheeling diodes remain reverse biased, and critical current levels are avoided by current limiting action of the VSC [39, 132].

To further analyze the fault characteristics of VSCs three different stages of fault response are identified: capacitor discharge, diode freewheeling and grid current feeding stage.

1. Capacitor discharge stage

DC link capacitor discharges immediately following a DC network fault as shown in Figure 4.1(b). Peak fault current at this stage could rouse up to several

times the nominal current depending on the capacitance of the DC link capacitor and fault loop impedance. Initial capacitor discharge current response of the network takes two forms depending on network damping [19]. For an undamped network, the current is defined as (4.1).

$$i(t) = \frac{V_{CF}(0)}{L\omega_d} e^{-\alpha t} \sin(\omega_d t) \qquad (4.1)$$

Where $V_{CF}(0)$ is the initial capacitor voltage and ω_d is the damped frequency defined as in (4.2),

$$\omega_d = \sqrt{\omega_0^2 - \alpha^2} \qquad (4.2)$$

Where, $\alpha = R/2L$ is the damping factor, and $\omega_0 = 1/\sqrt{LC_F}$ is the resonant frequency. Here, R and L are the resistance and inductance between fault and discharge capacitor.

2. Diode freewheeling stage

This stage is initiated when the DC link capacitor voltage reaches zero, and VSC current starts to commutate through the freewheeling diodes as shown in Figure 4.1(c). The fault current, i at this stage is defined by (4.3).

$$i = I_0 e^{-\left(\frac{R}{L}\right)t} \qquad (4.3)$$

Where I_0 is the initial fault current. The current at this stage could be several times the nominal current and can damage the freewheeling diodes if the fault is not interrupted within safe time limits.

3. Grid current feeding stage

At this stage, VSC acts as an uncontrolled diode bridge rectifier (see Figure 4.1(d)) and will continue to feed the fault through the freewheeling diodes of the VSC.

4.2.2. DC-DC converter post fault behavior

DGs connected to the DC bus feed the fault through interfacing converters. Figure 4.2(a) shows a DC-DC converter with a pole-pole fault.

Similar to VSCs, DC-DC converter capacitors contribute to the initial capacitor discharge current resulting in a quick V_{dc} drop. For low R_f values, if V_{dc} drops below converter output voltage, freewheeling diodes are forward biased. Inductor current will rise only to be limited by cable resistance. Fault current through the converter

will rise higher than the nominal current of the converter. The IGBTs will be blocked leaving the diodes exposed to fault currents.

The fault response of a DC-DC converter is similar to that of a VSC, and consists of three stages; capacitor discharge (see Figure 4.2(b)), diode freewheeling stage (see Figure 4.2(c)) and DG current feeding stage (see Figure 4.2(d)).

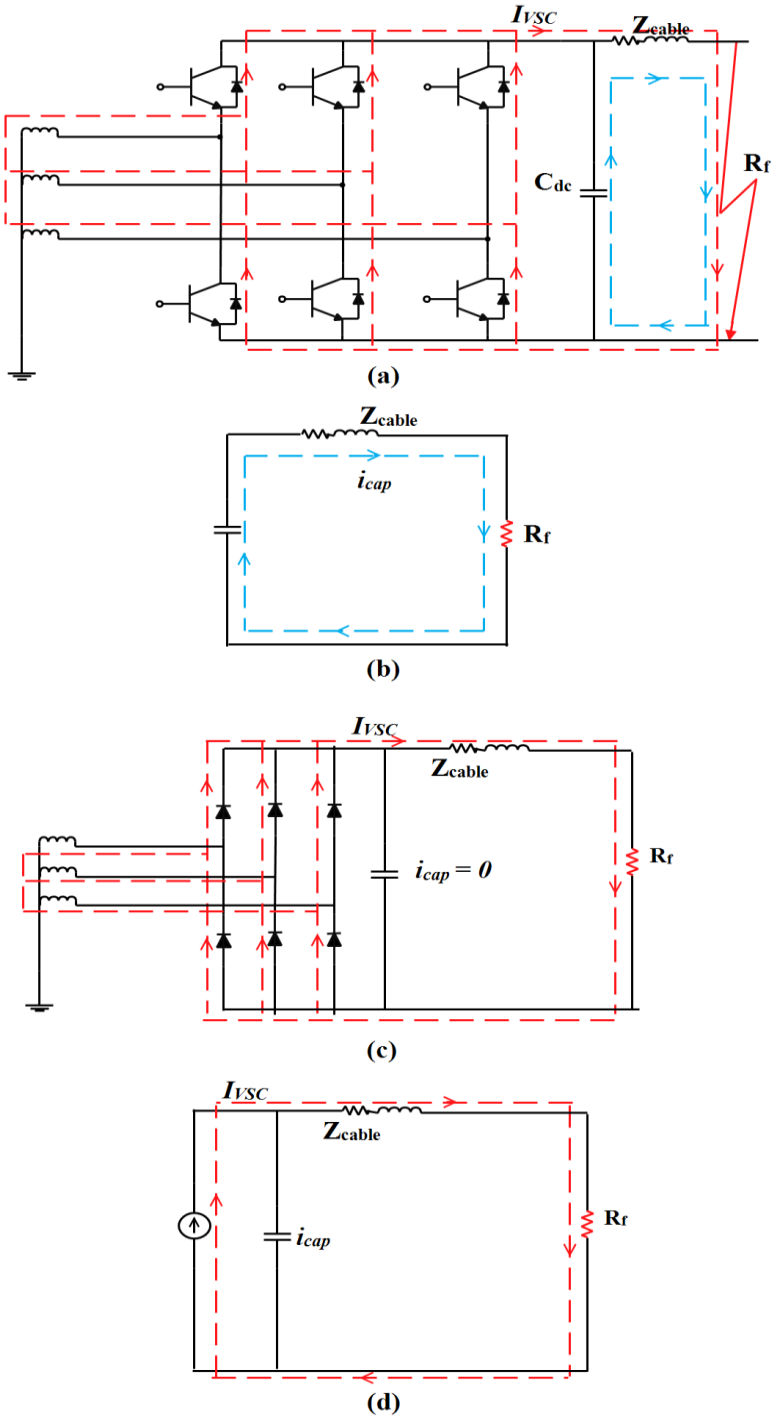

Figure 4. 1 (a) VSC with pole-pole fault, (b) equivalent circuit for capacitor discharge stage, (c) equivalent circuit for diode freewheeling stage, (d) equivalent circuit for grid current feeding stage.

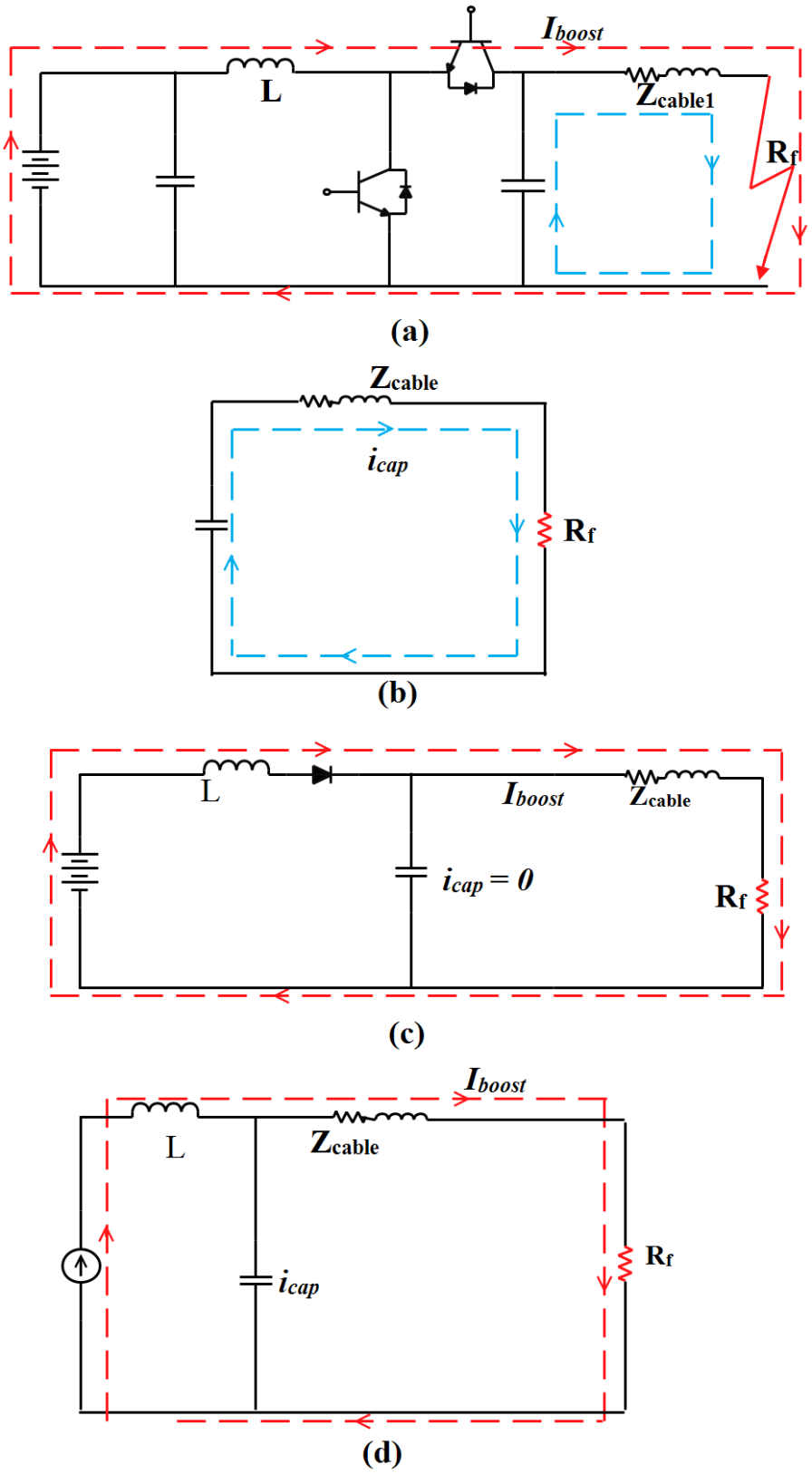

Figure 4. 2 (a) DC-DC converter under pole-pole fault, (b) equivalent circuit for capacitor discharge stage, (c) equivalent circuit for diode freewheeling stage, (d) equivalent circuit for DG current feeding stage

4.3.Pole –pole fault: overall system response

A pole-pole fault is the most critical fault in a DC network because of the resulting very high fault currents. Pole-pole fault on DC terminals of the network (see Figure 4.3), may be considered as an additional load with very low resistance being connected [25].

As discussed in Section 4.2, depending on fault impedance, fault location and fault type, interfacing converters in the network show a varying behavior. In this analysis DCMG network with AC grid side neutral point solidly grounded and DC bus ungrounded arrangement is employed. In Figure 4.3, transient and steady-state current paths in the considered DCMG network during a pole-pole fault are shown. Following the fault, capacitors discharge quickly causing the drop in V_{dc}. From the figure, utility grid, PV plant and ESS, all together contribute to the fault current. Current from these DGs increase rapidly and flow to the fault through converter free-wheeling diode paths. Hence, it is important to block all the fault current paths by employing breakers at the required locations. In Figure 4.4 the variation of DC line current, I_{dc} and DC bus voltage, V_{dc} under a pole-pole fault are shown. DC link capacitance discharge causes a transient current with high amplitude, and low rise time. This sudden capacitor discharge causes a sudden drop in DC bus voltage and as a result, converter freewheeling diodes are forward biased initiating the diode freewheeling stage of the converter. AC grid and interconnecting DGs will continue to feed through this freewheeling diode path the fault resulting in very high fault current magnitude as shown in Figure 4.3.

Pole- ground faults are a common occurrence in a power network. Fault response following a ground fault mainly depends on grounding configuration. Networks with different grounding configurations show different ground fault characteristics and are further discussed in Chapter 5.

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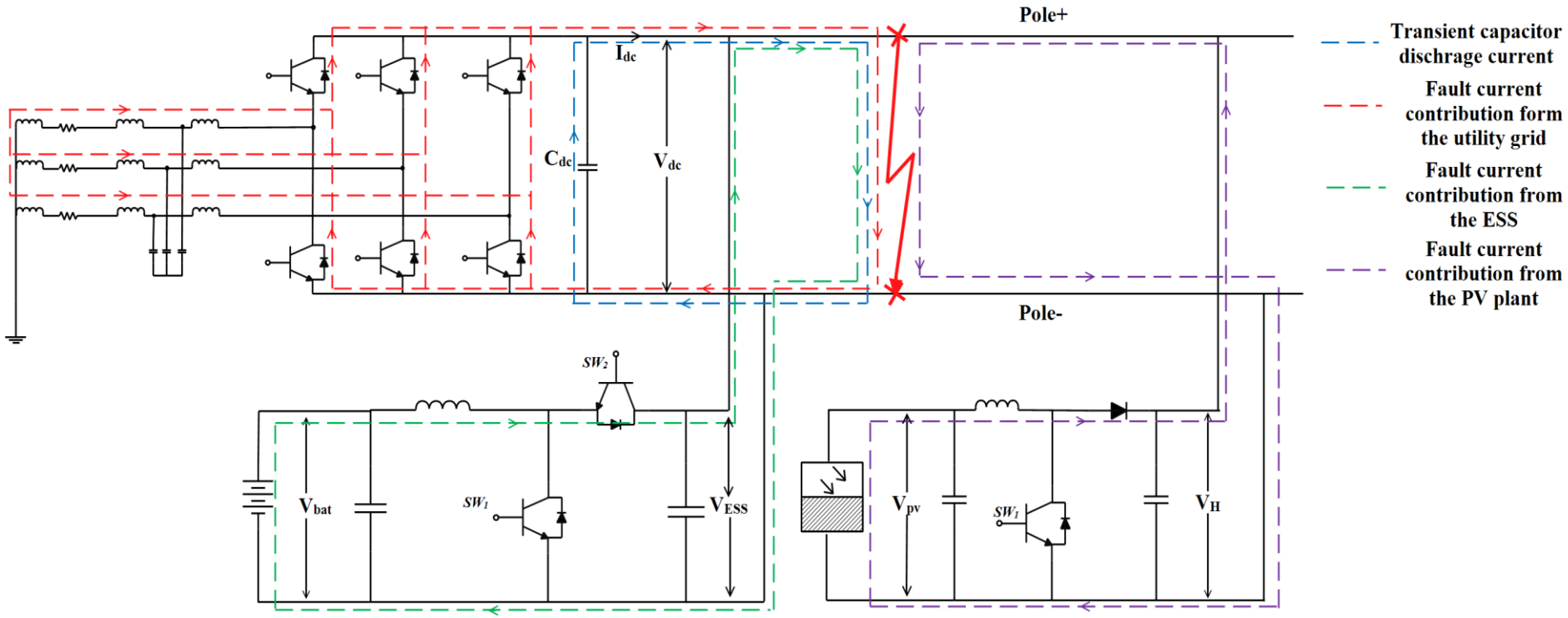

Figure 4. 3 Current flow paths in a DCMG network with a pole-pole fault

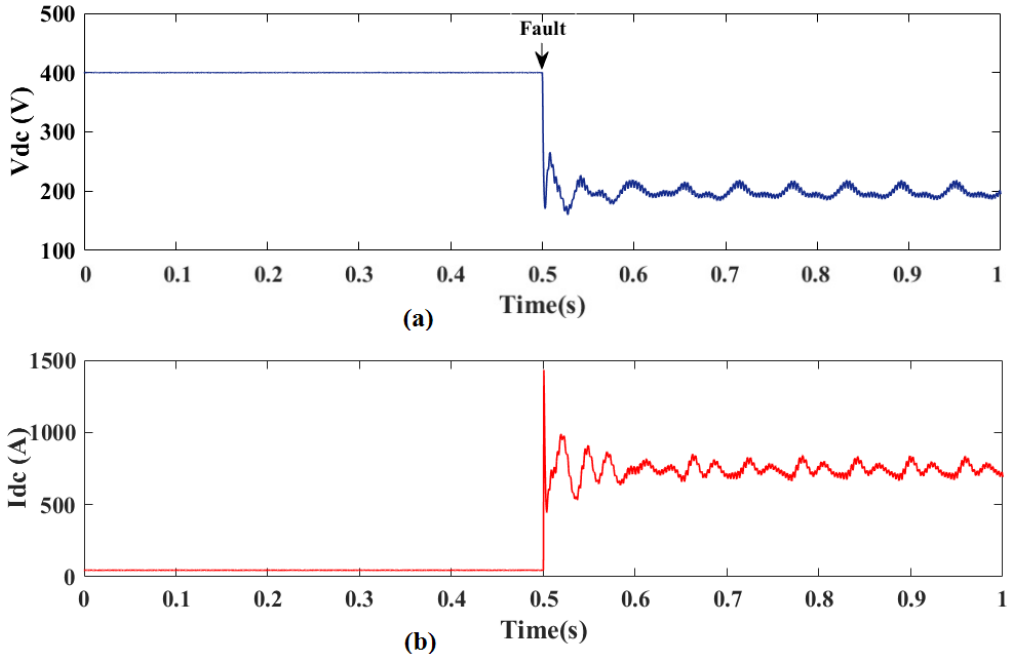

Figure 4. 4 Trend of (a) DC bus voltage , (b) DC line current , in a DCMG under a pole-pole fault

5. DC MICROGRID GROUNDING

To ensure protection against the hazards of electricity, power network grounding is an important necessity. Even though DC distribution networks have reached a level of maturity, certain aspects such as grounding of DC networks require further attention. This chapter explores the DC network grounding configurations that facilitate safer and reliable operation [133-134].

To contribute for a better understanding of DC network grounding, this chapter reviews different grounding configurations under different grounding design considerations.

5.1.Grounding design considerations in DC networks

Power network grounding is an important aspect in protection, which involves several design considerations:

1) Facilitating reliable ground fault detection.
2) Limiting touch voltages and fault currents to safe levels.
3) Limiting transient over-voltages and voltage fluctuations.
4) Facilitating ground fault ride-through capability.
5) Minimizing stray current induced corrosion.

Facilitation of safety for personnel and equipment is the main objective in the design of a grounding scheme. This requires the limiting of touch voltages and transient over-voltages [132-134].

Reliable ground fault detection capability is an important aspect to be considered in selecting a grounding scheme. Hence, the selection of ground fault detection scheme for a particular network is determined based on the grounding configuration employed in the network.

Solidly grounded networks features low touch voltage and immunity to transient over-voltages. However, these networks are unable to ride through faults. Hence, it is not suitable for certain applications, which require the system to continue operation without immediate shutdown. In contrast, high resistance grounded networks offer good fault ride-through capability, but may give rise to high touch voltages and transient over-voltages. These networks are prone to noise and disturbances. During a network disturbance, aggregated network to ground

capacitance and inductance may produce oscillatory over-voltages in reference to ground. This can have a detrimental effect on equipment and insulation [133].

Stray current induced corrosion is a major issue incorporated with DC networks. Taking necessary measures to limit stray current will prevent any structural damage due to stray current. High resistance grounding limits the flow of stray current; hence, it minimizes the issue of stray current induced corrosion. Conversely, in a solidly grounded network, there will be high stray current, and requires other measures to prevent stray current induced corrosion.

From the above discussion, it is clear that there are certain tradeoffs in the design of a DC network grounding configuration. Hence, to decide grounding configuration, certain design considerations are prioritized based on the application the network is being used for.

5.2.DC microgrid grounding methods

Grounding configurations for DC network system grounding are listed below [132-134]:

1) Ungrounded DC bus
2) High resistance grounding
3) DC bus solid grounding
4) DC bus midpoint solid grounding
5) Reconfigurable grounding

DC networks are interfaced with the utility grid at point of common coupling. AC utility grounding arrangement affects the selection of DC network grounding configuration. Possible DC network grounding configurations with AC grid grounding configurations: (i) solidly grounded AC utility network and (ii) ungrounded AC utility network, is discussed below.

5.3.1. Solidly grounded AC utility network

1. Ungrounded DC bus

Figure 5.1 shows the fault current paths in a DCMG network followed by a pole-ground fault in the DC positive pole. Pole-ground faults in the DC negative pole shows similar behavior. Hence, this analysis can be extended for pole-ground faults

in the DC negative bus. In this analysis different ground fault resistance values are used to analyze the impacts of low and high ground fault resistances. This study presents the network behavior under typical high and low ground fault resistances of 5 Ω and 0.1 Ω respectively.

A . High ground fault resistance (R_g=5 Ω)

During pole-ground faults with high fault resistance, V_{dc} is quickly brought back to nominal value by the G-VSC controls as can be seen from Figure 5.2(a). Figure 5.2(b) shows the trend of variation of potential between DC positive pole and ground, V_{pole+} with a ground fault. Ground current, I_g (see Figure 5.2(c)) shows a similar waveform and the frequency as V_{pole+} after the ground fault. The DC component of I_g passes through the freewheeling diodes as shown in Figure 5.1.

With high fault resistances, the direction of I_g current through the G-VSC is outward from the upper terminal of the G-VSC, I_{vsc+} (see Fig. 5.2(d)) and inward from the lower terminal, I_{vsc-} (see Fig. 5.2(e)). As for the PV plant current, I_{pv} and ESS current, I_{ess} there is no reclosing path for current to flow through the ground. The fault current path shown (i.e ground fault contribution of I_{pv} and I_{ess}) in Figure 5.1 do not exist under high resistance faults. Hence, ESS and PV plant do not feed the ground fault. They feed only the load current as shown in Figure 5.2 (f) and (g) (in the situation considered, I_{ess} = 0, as G-VSC regulates V_{dc} on its own and ESS do not take part in V_{dc} regulation).

The load current, I_{load} is contributed by G-VSC, PV plant and ESS, as defined by (5.1)

$$I_{load} = I_{vsc-} + I_{ess} + I_{pv} \qquad \textbf{(5.1)}$$

Here, I_{vsc-} is current through the lower terminal of the VSC, I_{ess} is current from ESS and I_{pv} is the solar PV current.

Current though the VSC upper terminal, I_{vsc+} is equal to the load current contribution and ground fault current as given by (5.2).

$$I_{vsc+} = I_{vsc-} + I_g \qquad \textbf{(5.2)}$$

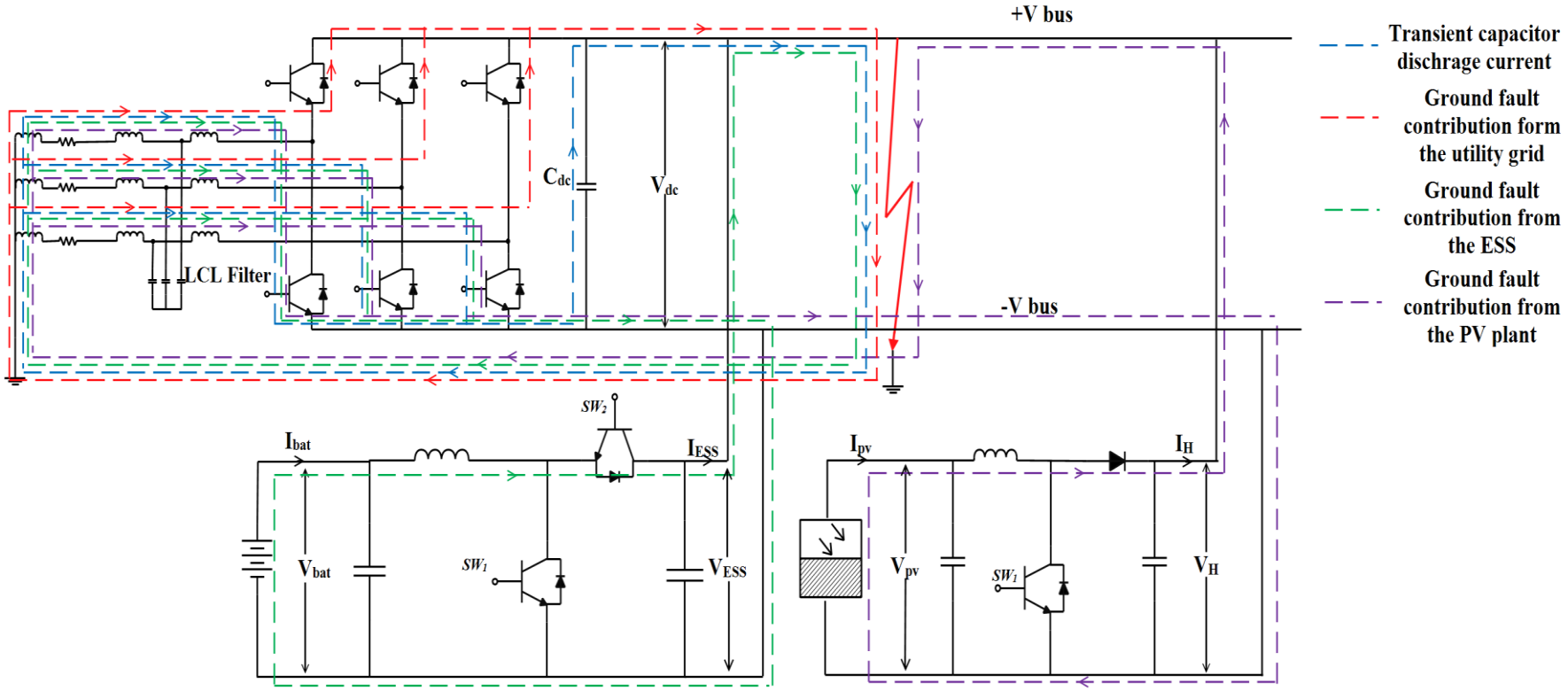

Figure 5. 1. Ground fault current flow paths in a AC grid transformer solidly grounded, DC bus isolated DCMG.

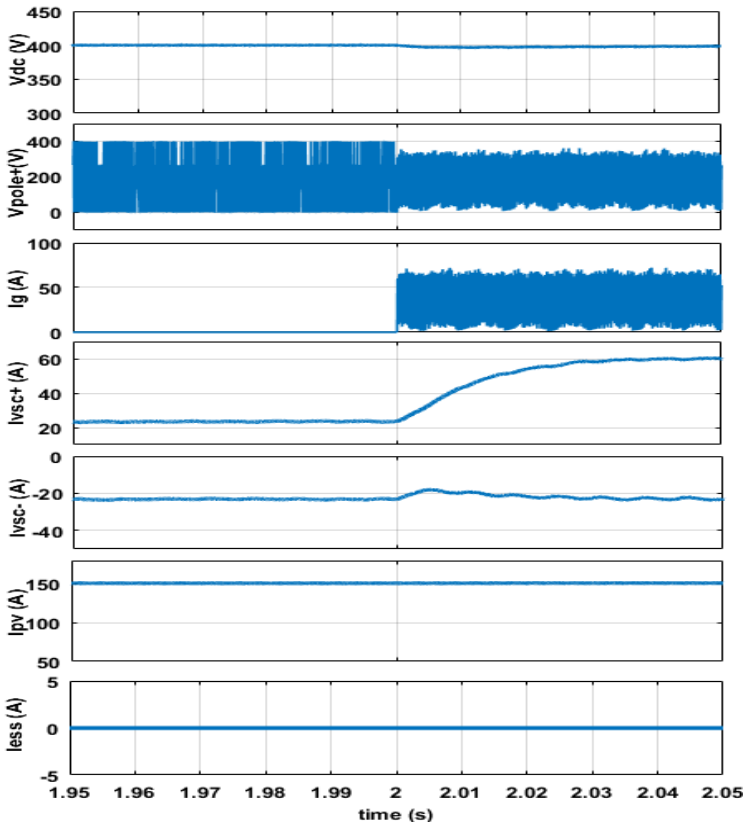

Figure 5. 2 Variation of (a) DC bus voltage, (b) voltage between DC positive pole and ground, (c) ground fault current, (d) current through upper terminal of VSC, (e) current through lower terminal of VSC, (f) PV plant current, (g) ESS current; at a high R_g ground fault in a DCMG with AC grid transformer neutral point solidly grounded and DC poles isolated.

With this grounding configuration (solidly grounded AC network and ungrounded DC Bus), ground fault detection techniques, which monitor $\boldsymbol{I_g}$ can be employed to detect high resistance ground faults. $\boldsymbol{I_g}$ in the range of few mA is easily detected by high sensitive ground fault current detection relays currently available. However, for very high $\boldsymbol{R_g}$ ground current is very low and cannot be detected, and requires advanced fault detection technique, such as insulation monitoring. Insulation monitoring techniques mostly uses current or voltage injection to identify drop in the insulation resistance as a result of ground fault.

B. Low ground fault resistance ($\boldsymbol{R_g}$=0.1 Ω)

From Figure 5.3 (a), it can be seen that $\boldsymbol{V_{dc}}$ is pulled out of nominal value. Figure 5.3 (b) and (c) shows the voltage variation between DC positive pole and variation of $\boldsymbol{I_g}$ respectively.

After the ground fault, V_{dc} drops instantly due to the discharge of the DC link capacitor, I_{cap} (see Figure 5.3 (d)). This capacitor discharge current passes through the G-VSC lower terminal as shown in the Figure 5.1. Even after the initial capacitor discharge V_{dc} varies rapidly since there is a capacitor ripple current, which flows through the capacitor.

For a low R_g, direction of DC component of current through the G-VSC is outward from both upper terminal (Figure 5.3 (e)) and lower terminal (Figure 5.3 (f)) of the VSC. Hence, for solar PV plant and ESS, unlike the earlier case considered, there exists a reclosing path for the fault current to flow as shown in Figure 5.1. Trend of I_{pv} (Figure 5.3 (g)) and I_{ess} (Figure 5.3 (h)) after the fault indicate both PV plant and ESS feed the ground fault in this scenario. Here, I_{vsc-} is the sum of ESS and PV plant ground fault current contribution and DC link capacitor ripple current. Ground current I_g is the sum of both I_{vsc+} and I_{vsc-} as given by (5.3).

$$I_g = I_{vsc+} + I_{vsc-} \qquad (5.3)$$

Here, I_{vsc+} is the current through the upper terminal of the VSC.

Detection of this type of fault is easy as it results in high ground current. However, isolating the fault currents within safe time and current limits is a challenging task associated with these faults. Normally, IGBT self-protection schemes such as DESAT protection activates within few µs, blocking off the IGBTs. This results in blocking of fault current path (i.e $I_{vsc-} = 0$). In that case there is no ground fault current from the ESS and PV plant. Even though the IGBT operation is cutoff by DESAT protection, fault current passes through the freewheeling diodes (in this case $I_g = I_{vsc+}$, which is still very high). Hence, suitable fault interruption equipment to isolate the fault is required.

From Figure 5.3(a) it can be seen that with this grounding configuration (solidly grounded AC network and ungrounded DC Bus) DCMG loses the ability to regulate the bus voltage; hence, it cannot ride through low resistance ground fault. It requires the fault to be isolated quickly to interrupt I_g flow. Another disadvantage of this grounding scheme is, it poses a threat to personnel and equipment due to high I_g flow.

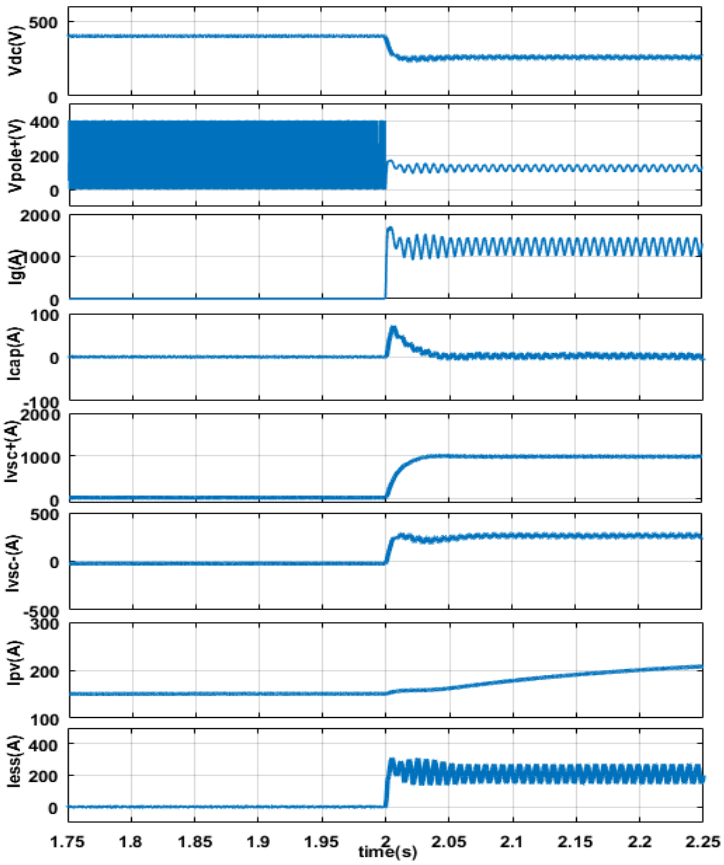

Figure 5. 3 Variation of (a) DC bus voltage, (b) voltage between DC positive pole and ground, (c) ground fault current, (d) capacitor discharge current (e) current through upper terminal of VSC, (f) current through lower terminal of VSC, (g) PV plant current, (h) ESS current; at a low R_g ground fault in a DCMG with AC grid transformer neutral point solidly grounded and DC poles isolated.

5.2.1. Ungrounded AC utility network

1. DC bus solid grounding

In a DC bus solidly grounded network, ground fault in the DC positive pole will be seen as an extra load with a low resistance by all DGs in the network. Figure 5.4 shows the fault current flow path during a ground fault in this network.

From Figure 5.4, a ground fault will effectively create a pole to pole fault in the network. Hence, the analysis of pole-pole faults under Section 4.3 is also valid in this scenario. As can be seen in Figure 5.4, G-VSC, ESS, PV plant and DC link capacitor current contribute for $\boldsymbol{I_g}$.

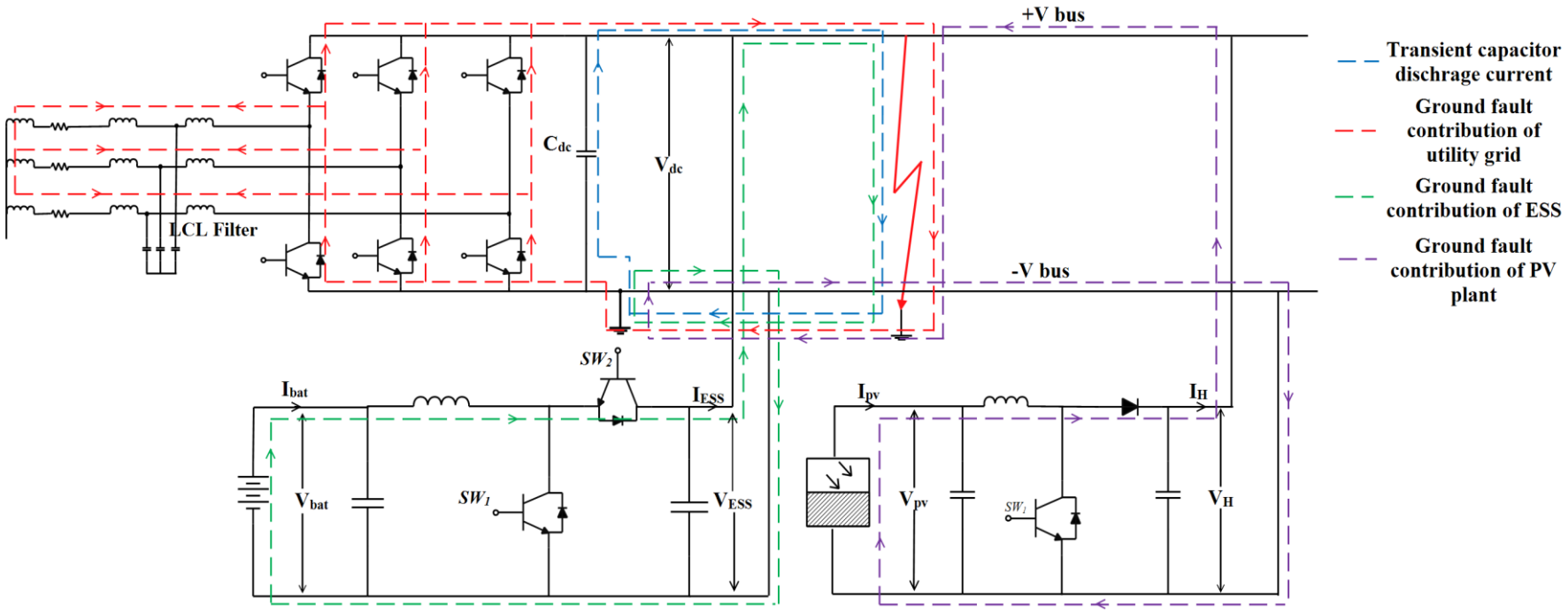

Figure 5. 4 Ground fault current flow paths in a AC grid transformer neutral isolated, DC negative bus solidly grounded DCMG.

A. High ground fault resistance (R_g = 5 Ω)

For high fault resistance, (R_g= 5Ω) simulation results are shown in Figure 5.5. Here, the fault is applied at t = 2 s. For a high R_g, if the sum of I_g and I_{load} is less than the total current that can be supplied from VSC, PV plant and ESS, DGs and network controls have the ability to maintain V_{dc} at the nominal. Figure 5.5 (a) shows the variation of V_{dc} following a ground fault in this network. As can be seen, V_{dc} is brought back to the nominal value by network controls. Capacitor discharge current, I_{cap} (Figure 5.5(f)), G-VSC current, I_{vsc} (Figure 5.5(c)), solar PV current I_{pv} (Figure 5.5(d)) and ESS discharge current I_{ess} (Fig. 5.5 (e)) and contributes for I_g (Figure 5.5 (b)). However, as seen in the Figure 5.5(e) VSC controls quickly restore V_{dc} and there is only very small ESS discharge current during the fault. Capacitor current component is shown in Figure 5.5(f) causes the reduction of V_{dc} immediately after the fault.

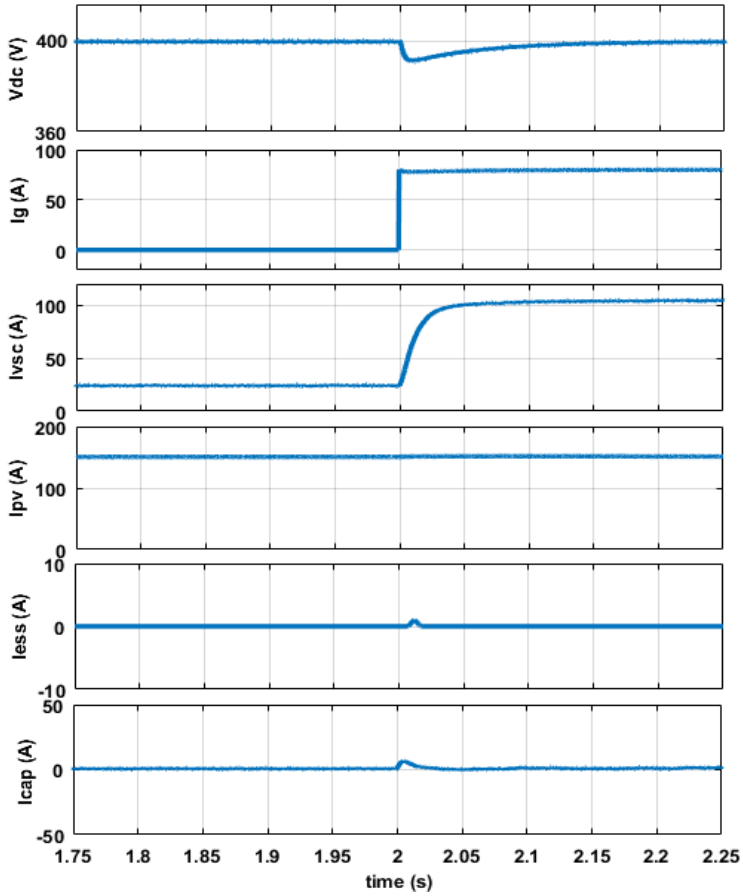

Figure 5. 5 Trend of variation of (a) DC bus voltage, (b) ground fault current, (c) VSC current, (d) PV current, (e) ESS current, (f) capacitor discharge current, with a high R_g ground fault in a DC negative bus grounded DCMG.

Fault detection technique based on I_g monitoring can be employed to detect faults with this grounding configuration. However, very high R_g give rise to very small ground current, which cannot be detected by normal ground current monitoring schemes. Hence, it requires a fault detection technique, such as insulation monitoring to detect these high resistance faults.

B. Low ground fault resistance (R_g= 0.1 Ω)

For low R_g values, I_g is higher than the maximum allowable current from the G-VSC, PV plant and ESS. Consequently, V_{dc} settles at a lower value than the nominal voltage (see Figure 5.6 (a)) following a fault.

As discussed under Section 4.2, V_{dc} determines the operational mode of the power electronic converters connected to the DC bus. When V_{dc} is pulled below $\mathbf{2\sqrt{2}V_{an}}$, the G-VSC operates in over-modulation and if V_{dc} is pulled below $\mathbf{1.35\sqrt{3}V_{an}}$, G-VSC works irregularly as a diode rectifier.

Ground fault current flow path is shown in Figure 5.6. The trend of variation of I_g (Figure 5.6(b)) shows that it reaches considerably high values (both capacitor discharge and steady state current values), without any limitation. The trend of I_{vsc} (see Figure 5.6(c)) shows that following a ground fault, the current through the G-VSC exceeds the current limit of the G-VSC. Hence, G-VSC is no longer operates in the modulation region. It starts to operate as a diode rectifier and fault current pass through the freewheeling diodes. Even the activation of self-protection blocking OFF the IGBTs is ineffective under this condition.

The trend of I_{pv} and I_{ess} following the fault are shown on Figure 5.6(d) and Figure 5.6(e) respectively. The DC/DC converter of ESS cannot limit the fault current through the converter as V_{dc} drops below the battery terminal voltage causing fault current to flow through the freewheeling diode of the converter. DC link capacitor discharge current, I_{cap} is shown in Figure 5.6 (f).

The analysis shows that, low R_g ground fault in a DC network with this grounding configuration (ungrounded AC network and solidly grounded DC Bus) can be easily detected due to the very high I_g. It can be seen from Figure 5.6 (a) that DCMG does not have the ability to ride through these low R_g ground faults with this network grounding configuration due to the loss of bus voltage stability. Fast fault detection and interruption techniques should be adopted to protect the personnel and equipment from high I_g.

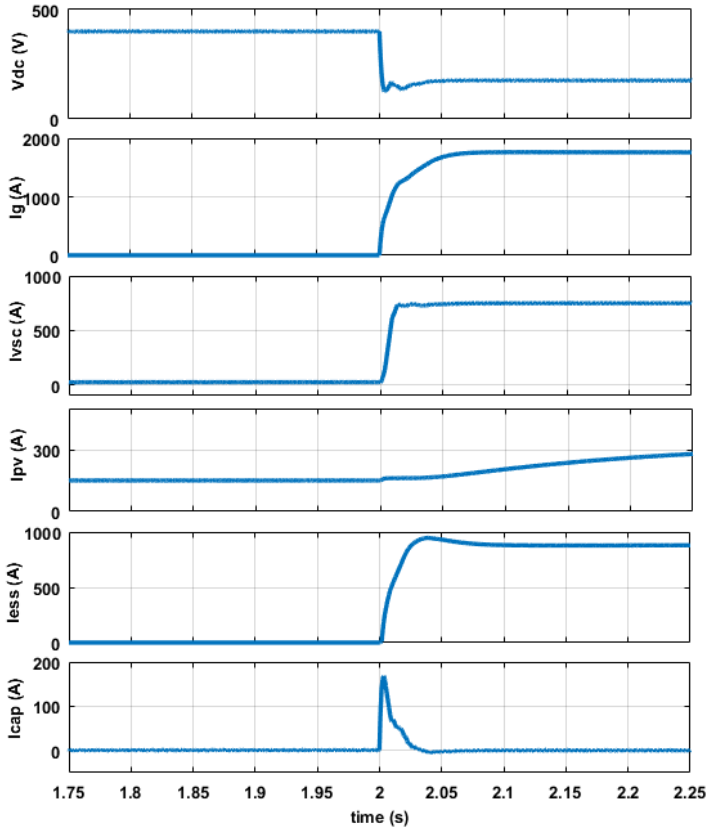

Figure 5. 6 Variation of (a) DC bus voltage, (b) ground fault current, (c) VSC current (d) PV plant current, (e) ESS current, (f) capacitor discharge current, at a low R_g ground fault, in a DC negative bus grounded DCMG

2. DC bus high resistance grounding

High resistance grounded network do not have a low resistance path for $\boldsymbol{I_g}$ to flow. This grounding technique enables fault ride-through capability. This inherent fault ride-through capability is the main advantage of this grounding configuration. Magnitude of $\boldsymbol{I_g}$ during a ground fault can be controlled by proper selection of grounding resistance to protect equipment and personnel. However, high grounding resistance makes it difficult to detect ground faults. In addition, a subsequent ground fault can create a pole-pole fault through the ground path causing severe damages.

In the selection of grounding resistance, tradeoffs between ground fault ride-through capability, ability to detect ground faults and ability to limit ground currents have to be made. In general, equipment can withstand few hundred ***mA*** of ground fault currents and for human protection it should be limited to 30 mA in accordance with IEC 479-1 [132]. Ground currents of few ***mA*** are easily detected by currently available high sensitive ground current detection relays. Grounding resistance is

selected such that ground fault causes modest current flow (to facilitate fault detection) independent of the R_g; but, is not high such that it affects the continuity of supply to the loads and pose a threat to equipment and personnel. Despite the ground fault ride-through ability, this grounding configuration has few drawbacks such as, it gives rise to large voltage spikes with respect to ground, and is largely influenced by disturbances and noise [133, 134].

The fault current flow path when the negative pole is high resistance grounded is similar to as in Figure 5.4. However, ground current magnitudes are smaller compared to solidly grounded system. Simulation results for a low impedance ground fault (R_g= 0.1Ω) is shown in Figure 5.7. A DC bus grounding resistance of 20 kΩ is selected for this simulation. The trend of V_{dc} shown in Figure 5.7 (a) indicates that the ground fault barely affects the network performance. I_g (see Figure 5.7 (b)) is very low (I_g = 20 mA) despite R_g being low. However, ground current flow can be detected by high sensitive ground fault current monitoring schemes. Both V_{pole+} and V_{pole-} could be at a higher potential compared to ground depending on the employed grounding resistance. Hence, it is essential for both poles be protected using interrupting equipment. V_{pole+} (Figure 5.7 (c)) is pulled to zero with the occurrence of a fault while V_{pole-}(Figure 5.7 (d)) reaches nominal V_{dc}.

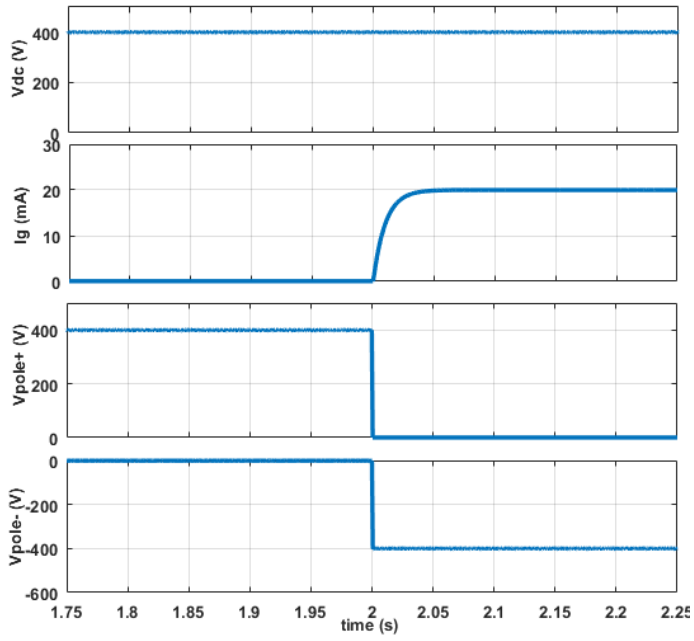

Figure 5. 7 Variation of (a) DC bus voltage, (b) ground fault current, (c) voltage between DC positive pole and ground, (d) voltage between DC negative pole and ground, at a low R_g ground fault in a DC bus high resistance grounded DCMG.

High resistance grounding schemes are commonly used in applications such as data center networks [133] and transit systems [134] due to its inherent fault ride-through capability, low I_g and low stray current [134]. Literature discusses the use of center-tapped grounding scheme and DC bus midpoint high resistance grounding [133], which are also currently used grounding configurations in such applications. Both these grounding configurations have advantages; enabling fault ride-through capability, low I_g and voltage shift based ground fault detection capability.

3. DC bus midpoint solid grounding

In a DC bus midpoint grounded network the potential of each pole is half the pole-pole voltage. Since both have potential with respect to ground, it is required to protect both poles of the network. DC bus midpoint is created using either capacitive or resistive dividing.

The transient ground fault current flow path following a ground fault in this network is shown in Figure 5.8. From Figure 5.8, in steady-state, neither G-VSC, ESSs nor PV plant contribute to the ground fault since there is no reclosing path for I_g to flow. Figure 5.9 shows the simulation results with R_g = 0.1 Ω. V_{dc} (Figure 5.9 (a)) can be maintained at nominal value regardless of the R_g value. Variation of I_g is shown in Figure 5.9 (b). I_g is contributed by G-VSC, ESS, PV plant and DC link capacitor discharge current.

From Figure 5.9 (c), during the ground fault in DC positive pole, V_{pole+} is pulled to zero irrespective of R_g value due to the DC positive pole capacitor discharge current I_{cap1} (Figure 5.9 (d)).

Transient fault current fed from G-VSC and ESS is shown in Figure 5.9(e) and Figure 5.9 (f) respectively. This fault current recloses at the negative pole capacitance (see Figure 5.8). With the transient current flow through the negative pole of the network, the voltage between negative-pole and ground, V_{pole-} will float and reach nominal bus voltage. This will allow the system to continue the supply of power (similar analysis is applicable for ground faults in the DC negative pole in a DC bus midpoint grounded system). Although these events are independent from R_g, the rate at which V_{pole+} is pulled to zero and V_{pole-} floats and reaches the nominal bus voltage depends on the value of R_g.

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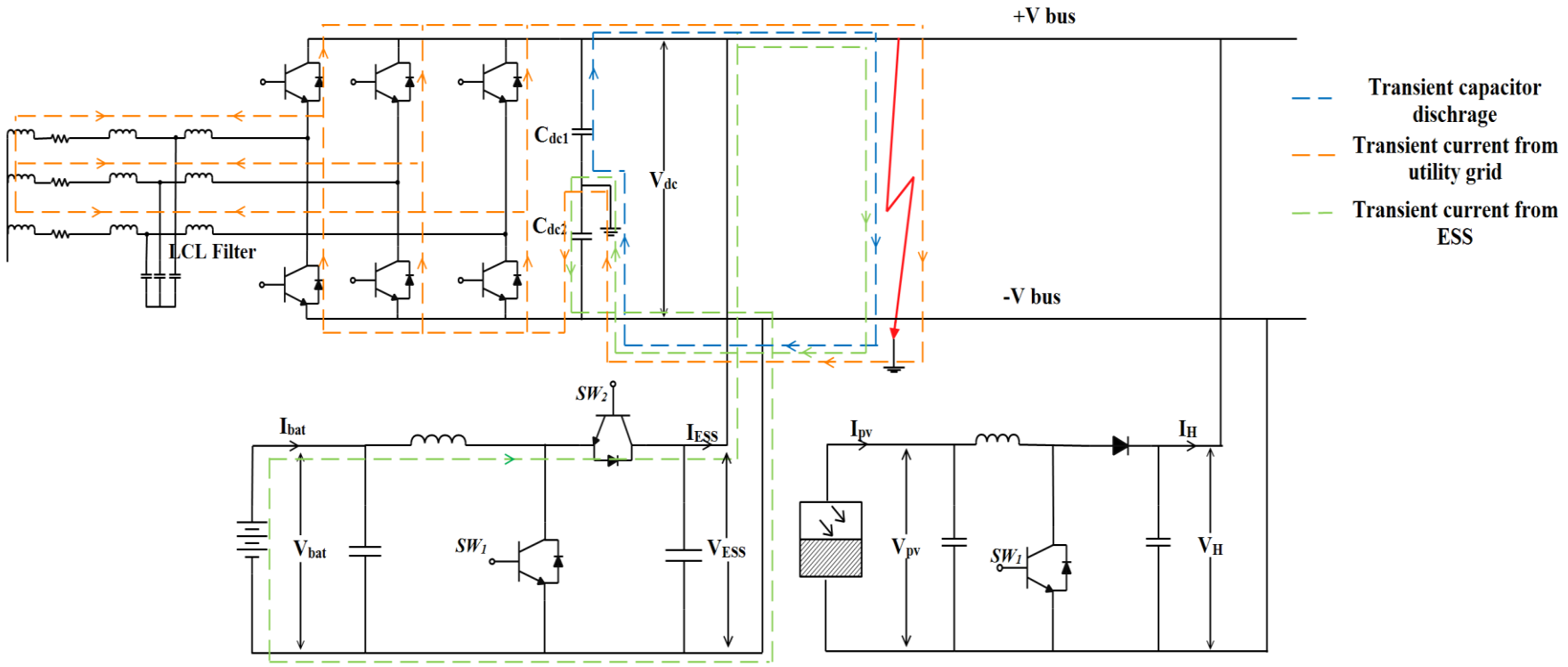

Figure 5. 8 Ground fault current flow paths in a AC grid transformer neutral isolated, DC bus midpoint grounded DCMG

Detection of ground faults in DC bus midpoint grounded systems is relatively easy utilizing the voltage shift in the poles of the network. The DCMG network is safe from ground fault currents in steady state. However, very low $\boldsymbol{R_g}$ can give rise to high $\boldsymbol{I_g}$ transient, which results due to capacitor discharging and charging. A possible solution is to ground the midpoint of the DCMG through a high grounding resistance to limit the magnitude of capacitor charge/discharge transient.

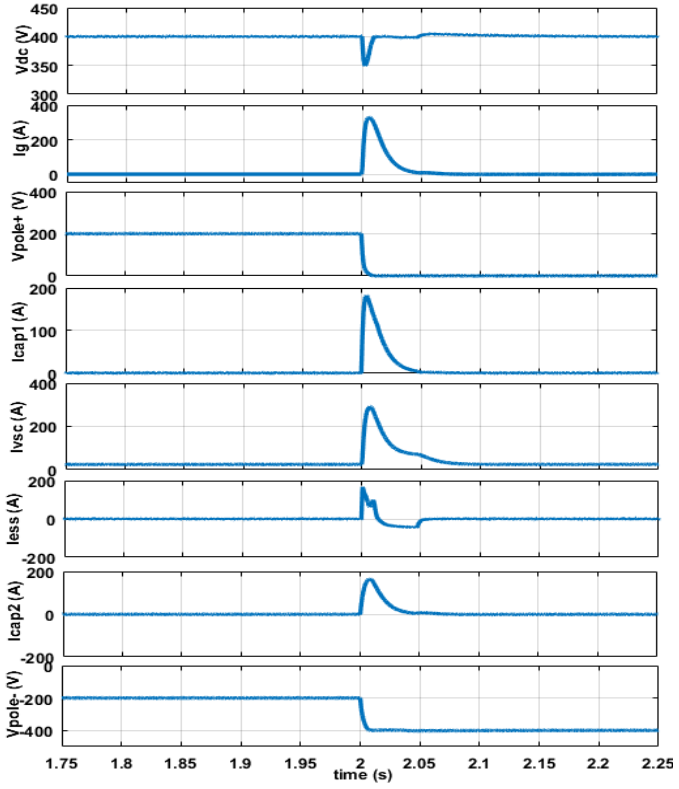

Figure 5. 9 Variation of (a) DC bus voltage, (b) ground fault current,(c) voltage between DC positive pole and ground, (d) capacitor discharge current (e) VSC current, (f) ESS current, (g) PV plant current, (h) voltage between DC negative pole and ground, at a low R_g fault in a DC bus midpoint grounded DCMG

When $\boldsymbol{R_g}$ is very high, voltage shifts slowly; hence take a long time to detect the ground fault using voltage shift based detection technique. Ground current measurement based fault detection schemes can also be utilized with this grounding configuration as capacitor discharging and charging currents results in a transient $\boldsymbol{I_g}$ component. The peak $\boldsymbol{I_g}$ value depends on ground fault resistance. Since $\boldsymbol{I_g}$ takes a small value for high $\boldsymbol{R_g}$ values, insulation monitoring devices must be used to detect these high $\boldsymbol{R_g}$ faults.

Currently DC bus midpoint grounding is used in data center/ telecommunication networks due to its inherent fault ride-through capability. Since this grounding configuration enables the fault ride-through capability, network can maintain power supply and is capable of regulating V_{dc} at nominal even in the presence of a ground fault.

4. Ungrounded DC bus

Ungrounded DC bus networks have an inherent fault ride-through capability during ground faults. It has a zero or very low I_g under a single ground fault [137]. However, second ground faults will create a pole-pole condition through the ground path, causing severe damage. Hence, the ground faults occurring in these networks should be cleared immediately.

Ground current detection devices cannot detect ground faults in these networks; hence, require more sensitive ground fault detection technique such as insulation monitoring, where AC/DC voltage injection is used to measure the system response [31, 138-140].

The main disadvantage of an ungrounded network is bus voltage can reach an elevated level with respect to the ground posing a danger to the public. Susceptibility to noise and disturbances in the network could give rise to under-damped transient over-voltages in these networks, which leads to deterioration of insulation and can damage the network equipment [31].

5. Reconfigurable grounding

When selecting a grounding configuration for a DCMG, minimizing stray current and avoiding unsafe over-voltages are two contradictory requirements. Different from the DC network grounding methods discussed earlier, in [141] reconfigurable grounding methods for DC traction networks are proposed. In this grounding configuration the network is operated in ungrounded configuration to reduce stray current induced corrosion. Upon the detection of a high voltage, the network is grounded through a power electronic switch to reduce the bus voltages to safe levels.

Reconfigurable grounding techniques are mainly proposed for DC traction networks to reduce the stray current [142, 145]. The use of reconfigurable grounding

configurations for DCMG networks has not been explored yet and requires further investigation.

• Diode grounding

Diode grounding is the solid grounding of DC bus through a diode circuit as shown in Figure 5.10(a). In this grounding configuration the current is allowed to flow from the ground towards the negative bus, if the voltage across diode increases above forward bias voltage. This grounding configuration also facilitates ground faults to be easily detected by ground current monitoring relays. For a small voltage between ground and the negative pole, the diode would conduct, resulting in high stray currents. Hence, in this grounding configuration the problem of stray current induced corrosion is not completely eliminated. [134, 141-143]. In [134], a reversed diode grounding configuration is proposed to eliminate the issue with the stray current. By placing the diode in reverse direction, stray currents are blocked, and at the same time, transient over-voltages created in the network are diminished.

• Thyristor grounding

Thyristor grounding shown in Figure 5.10(b) offers more control over the grounding configuration compared to diode grounding configuration. In this configuration, if the ground to negative bus potential rises above a preset value, thyristor gate is automatically triggered to ground the DC bus [141,142]. Ability to maintain DC bus ungrounded, minimizing the stray current [141,144] is the main advantage of thyristor grounding compared to diode grounding configuration. For better comparison and to summarize the analysis above, different DCMG grounding configurations and their operation features are provided in Table 5.1.

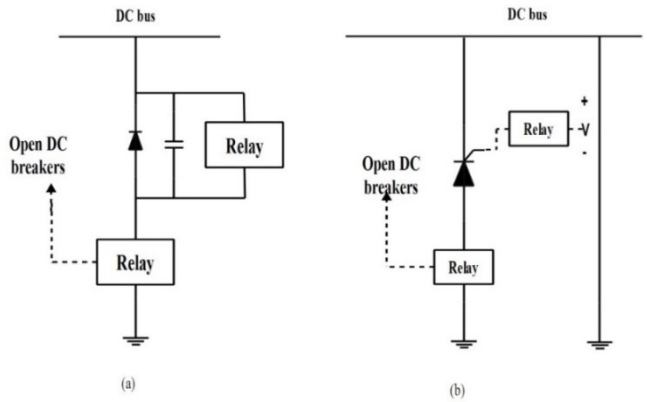

Figure 5. 10 (a) Diode grounding configuration; (b) Thyristor grounding configuration

Table 5. 1 DC microgrid grounding configurations, and their characteristic features.

DC network grounding configuration	**Applicability of fault detection schemes**	**Capability to ride-through ground faults**	**Ground fault current magnitude**	**Stray current**	**Transient over-voltages**	**Remarks**
Neutral point of AC side transformer **solidly grounded**, DC bus **ungrounded.**	• Ground current detection. • Insulation monitoring	No	High	High	Low	• Fault detection is relatively easy.
Neutral point of AC side transformer **ungrounded**, DC bus **solidly grounded.**	• Ground current detection • Insulation monitoring	No	High	High	Low	• Fault detection is relatively easy.
Neutral point of AC side transformer **ungrounded**, DC bus **ungrounded.**	• Insulation monitoring.	Yes	Very low	Low	High	• Ground faults must be cleared quickly to prevent subsequent ground fault creating a pole-pole fault through ground path
Neutral point of AC side transformer **ungrounded**, DC bus **high resistance grounded**.	• Ground current detection • Insulation monitoring.	Yes	Moderate	Moderate /low	High/ Moderate	• Low resistance grounding can be employed to prevent high transient overvoltages during disturbances in the network.
Neutral point of AC side transformer **ungrounded**, DC bus **midpoint grounded**.	• Detection of pole voltage shift. • Ground current detection. • Insulation monitoring	Yes	low (only a transient I_g)	High	Low	• Reduces requirements for insulation as touch voltage is half the nominal voltage. • Both poles require Protection.
Neutral point of AC side Transformer **ungrounded**, DC bus midpoint **high resistance grounded**.	• Detection of pole voltage shift. • Ground current detection. • Insulation monitoring	Yes	Low	High	High	• Limits the transient capacitor discharging/ charging current.
Neutral point of AC side Transformer **ungrounded**, DC bus **reconfigurable grounding.**	• Ground current detection. • Insulation monitoring	No	High	Moderate /low	Moderate /low	• Diode grounding cannot completely eliminate the stay current induced corrosion. • Reverse diode grounding is proposed to eliminate the issue of stray current. • Thyristor grounding scheme enables the operation in both ungrounded and grounded configurations.

5.3. Grounding system design: discussion

From the above study, it is clear that different tradeoffs have to be taken into consideration when deciding a suitable grounding configuration for a particular application. A wide system study is required in deciding the appropriate DCMG grounding configuration, and ground fault detection technique should be selected accordingly. Proper selection of DCMG grounding configurations could facilitate safety of the personnel by maintaining touch voltages and ground currents at safe levels. Most of the network equipment being power electronic devices, they are vulnerable to network transients and over-voltages. Hence, the prevention of network transient over-voltages is a crucial requirement, which can be addressed by the proper grounding of the network. Furthermore, the selection of the grounding configuration could facilitate reliable fault detection and ground fault ride-through capability under fault situations.

6. DC MICROGRID FAULT DETECTION AND CLASSIFICATION SCHEME

6.1. Background

Several DCMG fault detection schemes were reviewed in Chapter 2. From the discussion, it was identified that only the communication based fault detection scheme could provide fault localization capability. However, these communication based methods have demerits such as increased cost, the requirement for synchronized measurements and increased complexity.

This chapter proposes a fast and reliable scheme for the detection and isolation of faults in DCMG using the transient signals generated during the faults.

6.2. Proposed algorithm for fault detection and localization

The proposed fault detection and localization scheme is based on the hypothesis that the transient signatures generated during the fault events contain information on the occurrence of faults. These characteristic features can be extracted to develop a fault classification scheme, which can distinguish fault occurrences from other network disturbances. However, these DCMG fault features are not directly distinguishable. Therefore the network signals are preprocessed to extract fault features which are then used for fault classification. The proposed scheme for DCMG fault detection is illustrated in Figure 6.1.

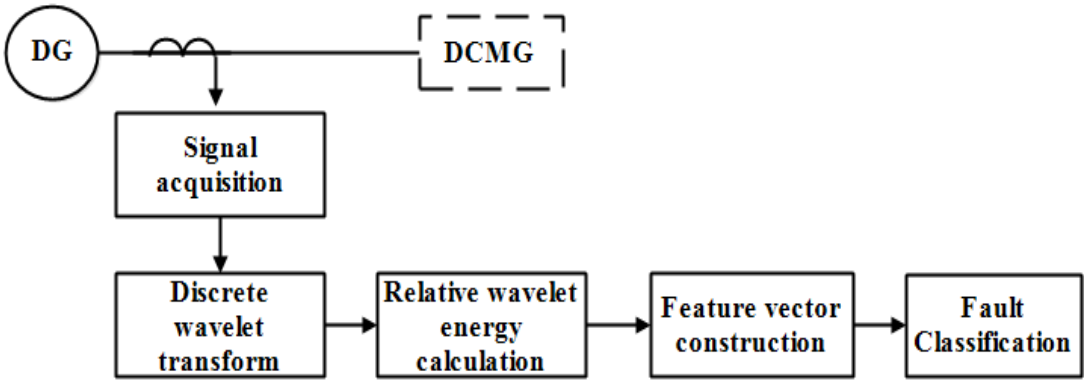

Figure 6. 1 Basic structure of the proposed DCMG fault detection algorithm.

Monitored signals are sampled for acquisition and discrete wavelet transform (DWT) is used to decompose the signal into frequency bands localized in time.

Time variation of relative wavelet energy (RWE) in the DWT decomposition levels are acquired using time series data embedding to construct the feature vector, and it is discussed in Section 6.4. Extracted features from the signals will be used to detect and classify faults using a pre-trained feed-forward ANN. Use of ANN for fault detection and event classification will be further discussed in Section 6.5.

6.3. Proposed protection coordination strategy

An effective protection coordination strategy minimizes the critical fault clearing time, enables quick system restoration and fault ride-through capability, and minimizes outages; thereby, it ensures the reliability and safety of the network [11]. Protection coordination issues bring many challenges: the selection of protection equipment to optimize the fault clearing with minimum outages, and miscoordination between devices are among these [20].

This Section presents the proposing protection coordination strategy to be deployed with the proposed fault detection and localization scheme. As shown in Figure 6.2, the network is segmented into several zones by selective positioning of DC circuit breakers, and these breakers in conjunction with digital relays operate to isolate the faulty zone, in the event of a fault. Backup protection is also implemented for the relevant relays and circuit breaker failures to improve system reliability.

The proposed fault detection scheme can be implemented and executed by digital relays monitoring the branch current signals at each branch, as shown in Figure 6.2. Table 6.1 summarizes the proposed coordination strategy between relays, to provide primary and backup protection to different components of the network from pole-ground and pole-pole faults, occurring at different locations of the network. For the faults occurring at load feeders, it is important to isolate the faulted load feeder to protect the other components in the network. Relays R_4, R_5, R_6 and R_7 provide primary protection against faults occurring in each load feeder (zones 2, 3, 4 and 5). The primary protection zones of the DCMG model are shown in Figure 6.2. For the faults occurring at the zone 1, relays R_1, R_2, and R_3 picks up the fault (primary protection), and fault current contribution from the utility grid, solar PV and battery storage is cutoff by DC circuit breakers. Relays R_1, R_2, and R_3 provide backup protection against faults occurring in zones 2, 3, 4 and 5, in case of breaker or relay failures at the load feeders.

The proposed protection coordination strategy is implemented using two types of time graded relays, rendering selectivity in fault interruption, and is discussed in later Sections.

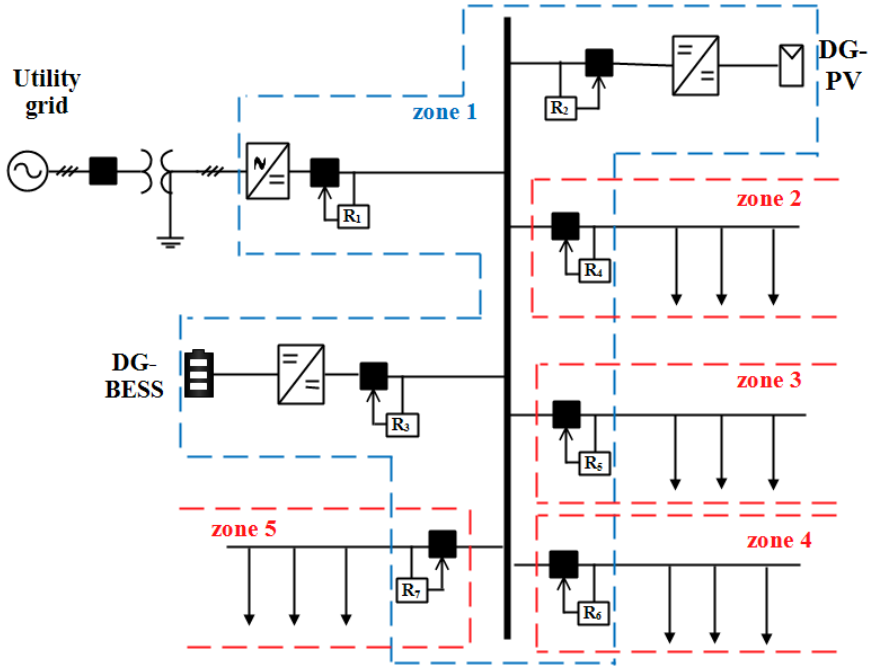

Figure 6. 2 Schematic of the notional DC microgrid model and the protection zones

Table 6. 1 DCMG fault locations and corresponding protection devices selected for the protection of DCMG network components.

DCMG Component	Primary protection		Backup protection	
	Dc bus faults	**Lateral feeder fault**	**DC bus fault**	**Lateral feeder fault**
Power converter protection	DC circuit breakers and Relays R_1, R_2 and R_3	DC circuit breakers, and relays R_4, R_5, R_6 and R_7	None	DC circuit breakers and relays R_1, R_2 and R_3
Battery protection	DC circuit breakers and relay R_3	DC circuit breakers and relays at R_4, R_5, R_6 and R_7	None	DC circuit breakers and relay R_3
Solar PV protection	DC circuit breakers and relay R_2	DC circuit breakers and relays R_4, R_5, R_6 and R_7	None	DC circuit breakers and relay R_2
Load Feeder protection	None	DC circuit breaker and relays R_4,R_5, R_6 and R_7	None	DC circuit breakers and relays R_1,R_2 and R_3

6.4. Signal processing and fault feature extraction

Signal processing based techniques are commonly adopted in identifying power system events. The use of signal processing allows extracting useful features contained in measured signals, in order to identify network events more effectively.

Fast Fourier transform (FFT), short time Fourier transform (STFT) and wavelet transform (WT) are commonly used signal processing techniques in analyzing signals. Although FFT offers very good frequency resolution, lack of time resolution in FFT makes it difficult to be used for transient signal analysis. This limits the use of FFT based methods for power system protection. The STFT, which analyses the signal in both time and frequency domains, is being widely studied for power system protection applications [42,148]. However, capabilities of STFT for signal processing is limited due to constraints on window size, as explained by the Heisenberg uncertainty principle [149]. i.e wide time window will result in particularly good frequency resolution but poor time resolution. Conversely, narrow time window will result in poor frequency resolution but, good time resolution. The WT has the capability to decompose a time-frequency signal into specific time-frequency resolutions. Hence, WT offers better time and frequency resolution compared with STFT and FFT techniques. Wavelet representation of a signal provides a portrayal of the variation of the frequency content with time, and hence reveal when and what type of transients take place in the signal. Wavelet analysis techniques have been proposed extensively for several power system applications, including fault classification and network event recognition [150-153].

6.4.1. Wavelet theory and multi-resolution analysis.

The Wavelets are generated from unique admissible wavelet $\psi(t)$, called mother wavelet, by scaling and translation along the time axis and is defined by (6.1), where, a and b are the scaling and translation parameters respectively.

$$\psi_{(a,b)}(t) = \frac{\psi}{\sqrt{a}}\left(\frac{t-b}{a}\right) \qquad (6.1)$$

The continuous wavelet transform (CWT) is defined as the correlation between the signal, $f(t)$ with a set of family wavelet $\psi_{s,\tau}(t)$ as defined in (6.2), where, $\psi^{*}_{(a,b)}(t)$ denotes its complex conjugate.

$$W_{(a,b)}(t) = \int_{\infty}^{-\infty} f(t)\, \psi^{*}_{(a,b)}(t)dt \qquad (6.2)$$

In principle, CWT provides a redundant representation of the signal under analysis. To overcome data redundancy and reduce calculation time, discrete wavelet transform (DWT) has been introduced, where wavelets are scaled and translated into discrete steps.

The DWT is performed by discretizing ***a*** and ***b***. Typically, these parameters are set to powers of 2, so that sampling of the frequency axis corresponds to dyadic sampling as in (6.3), where $\varphi_{(j,k)}$ are the wavelet detail coefficients at decomposition level ***j*** and location ***k***.

$$\psi_{(j,k)}(t) = \frac{\psi}{\sqrt{2j}}\left(\frac{t}{2^j} - k\right) \qquad (6.3)$$

6.4.2. Multi-resolution analysis

For most functions, wavelet transforms do not have an analytical solution. They can only be solved by numerical approaches. The multi-resolution analysis framework for the portrayal of a signal at different scales is introduced in [11, 154]. Given a signal ***f(t)***, its multi-resolution analysis up to level ***M*** is defined as (6.4)

$$f(t) = \sum_k a_{M,k} \frac{\psi}{\sqrt{2^M}}\left(\frac{t}{2^M} - k\right) + \sum_{k}^{M}\sum_k d_{j,k} \frac{\psi}{\sqrt{2^j}}\left(\frac{t}{2^j} - k\right)$$

$$\triangleq A_M(t) + \sum_j D_j(t) \qquad (6.4)$$

Here, $a_{M,k}$ are the approximation coefficients at level ***M***, and ***ψ(t)*** is the scaling function. The multi-resolution analysis decomposes the function ***f(t)*** into approximation coefficients, $A_M(t)$ and a set of detail coefficients, $D_j(t)$ as defined in the equation above [11,154].

According to this approach, DWT can be considered as a filter bank as shown in Figure 6.3, where DWT is performed by passing the sampled signal ***x(n)*** through high pass filter, ***h(n)*** and a low pass filter, ***g(n)*** and output is decimated by 2 to compute both approximation coefficients, $A_M(t)$ and detail coefficients, $D_j(t)$. Here, $A_M(t)$ represents output through the low pass filter, while $D_j(t)$ represents output through the high pass filter. Assuming the signal sampling frequency to be ***f***, the output frequency bands of decomposition levels are shown in Figure 6.3.

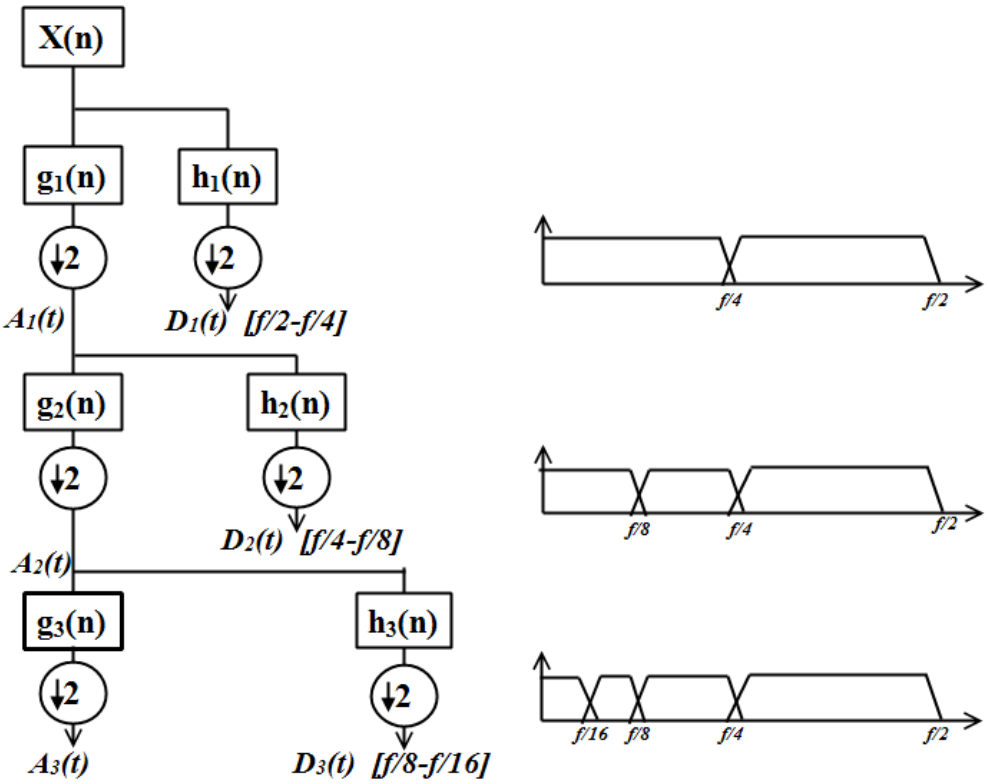

Figure 6. 3 DWT decomposition of signal with iterated filter banks, and frequency bands of different decomposition levels

6.4.3. Signal pre-processing

Good time and frequency resolution of wavelet transformation makes it possible to capture the abrupt changes of signals and localize the occurrence of high frequencies in the time domain. Selection of parameters such as, mother wavelet and decomposition level have a major impact on feature extraction process.

1. Selection of mother wavelet

In this study the selection of mother wavelet was based on the ability of the mother wavelet to capture intricate features of the fault signal and accuracy of the classification results, using a trial and error approach. Accordingly, db5 mother wavelet was selected as it provided the optimal performance in fault detection and localization in preliminary studies.

2. Selection of Decomposition level

The decomposition level is another parameter that affects the signal feature extraction process. Decomposition level is selected to capture all the high-frequency

content contained in the signal that is necessary for feature comparison. Higher the decomposition level higher will be the information extracted. However, higher decomposition level will result in longer temporal window for RWE calculation, which in turn results in longer classification time [155]. So, there is a tradeoff between the amount of information extracted and calculation time delay, which must be addressed. In this study the current signal is decomposed into 6 levels of decomposition for feature extraction. With the sampling frequency of 50 kHz, frequency bands of the high-frequency components captured by each decomposition level are shown in Table 6.2. MATLAB code for DWT decomposition of signals is provided in Appendix A.

Table 6. 2 Frequency bands of DWT decomposition levels, and minimum window size for RWE calculation in each decomposition level

DWT decomposition level	**Frequency bands (Hz)**	**Minimum window size for RWE calculation**
1	25 k - 12.5 k	0.04 ms
2	12.5 k - 6.25 k	0.08 ms
3	6.25 k - 3.125 k	0.16 ms
4	3.125 k -1.5625 k	0.32 ms
5	1565.5 - 781.25	0.64 ms
6	781.25 - 390.62	1.28 ms

6.4.4. Relative wavelet energy as an information tool

Monitored signals are sampled at sampling frequency of 50 kHz and discrete wavelet transformed (DWT) to decompose the sampled current signal into varying frequency bands, which are very well localized in time. The output of DWT multi-resolution analysis is a set of detail coefficients. The use of raw set of detail coefficients for classification requires a large memory space and processing time. Furthermore, the classification accuracies resulting from direct use of detail coefficients are rather poor. Hence, an information tool with reduced quantities, but without losing the properties of the original signal is required for the reduction of the number of features. Relative wavelet energy (RWE) within a selected time window is used in this study as the information tool for feature extraction.

The concept of wavelet energy is linked to the usual notions derived from Fourier theory [156,157]. The energy of the detail coefficients for a selected temporal window within a decomposition level can be defined as in (6.5).

$$E_j = \sum_K \left| d_j(K) \right|^2 \qquad (6.5)$$

Here, j is the decomposition level considered, K is the discrete time location, d_j is the wavelet coefficients and E_j wavelet energy of the j^{th} decomposition level. A sliding window can represent the variation of wavelet energy of a decomposed signal at each decomposition level [156].

The total wavelet energy, E_{Tot} of all the decomposition levels can be obtained using (6.6).

$$E_{Tot} = \sum_j \sum_K \left| d_j(K) \right|^2 \qquad (6.6)$$

The RWE, given by (7.7) yields the probability distribution of the wavelet energy at different decomposition levels $j=1,2,\ldots.n$.

$$RWE_j = {E_j}\Big/{E_{Tot}} \qquad (6.7)$$

Variation of RWE_j with time is a time scale probability density function. The RWE has demonstrated its effectiveness in detecting and classifying specific power system events [157-159]. In the proposed scheme, to follow the temporal variations of RWE, wavelet coefficient series, $\{d_{j,k}\}$, is divided into non-overlapping temporal windows of equal length.

To have a good time resolution for the proposed scheme, the smallest possible time window for RWE calculation is selected. There is a limit to the time resolution due to the frequency resolution, which depends on the selection of decomposition level. This concept is supported by Heisenberg uncertainty principle [149]. Consequently, the number of decomposition levels employed determines the smallest possible temporal window that should be selected to follow the temporal variations of RWE. In Table 6.2, the minimum window size to capture the high-frequency components within each decomposition level are given. The current signal is decomposed into 6 decomposition levels (see Section 6.4.3) in the proposed scheme. Hence, the minimum window size is selected as 1.28 ms.

6.4.5. Sliding window technique for feature vector construction

The majority of classifier models including ANNs overlook the temporal dependencies of the training data. The data correlation in the time domain is crucial in identifying the network events, as most of them are dynamic in nature [50]. In the proposed scheme, a shift register of delays is applied, where successive data of the time series is retained. It allows using the time-series data as a spatial vector which is an input into the classifier. This allows the classifier to capture the temporal dependencies in the input data. Hence, it enables a more accurate classification. This implicit transformation of time series data into a spatial vector is called sliding window technique, and is a widely recognized technique used to classify and predict events using temporal data [160-161].

As shown in Figure 6.4, at each instant **t**, the time series data can be truncated to the previous ***d*** number of samples to formulate the feature vector for the classifier. Here, ***d*** is the number of previous data windows employed to construct the feature vector [161].

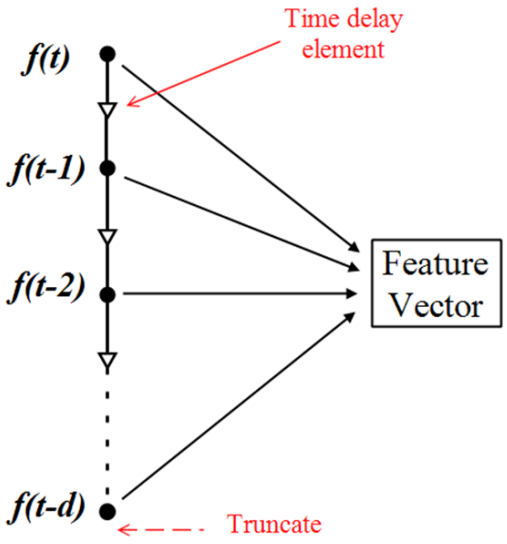

Figure 6. 4 Sliding window technique to construct a spatial vector using temporal data

6.4.6. Feature vector construction

The previous number of data windows for feature vector construction, ***d*** was selected on the basis of fault detection accuracy and ability to maintain proper

coordination between two types of relays. The initial studies showed that the classification accuracies improve with increasing values of ***d***. However, increasing values of ***d*** mean longer embedding time delay, resulting in longer fault detection time. This tradeoff between classification accuracy and speed of detection must be considered in the selection of ***d***.

To maintain coordination between relays, load feeder primary protection relays (relays R_4, R_5, R_6 and R_7) are required to operate prior to load feeder backup relays (relays R_1, R_2 and R_3). Hence, in the proposed scheme relays are time graded such that relays R_4, R_5, R_6 and R_7 operates prior to the relays R_1, R_2 and R_3. This time grading allows the relays R_1, R_2 and R_3 to back up the relays R_4, R_5, R_6 and R_7.

For *type I* relays, $\boldsymbol{d} = 2$ is employed. In order to allow proper time discrimination between upstream and downstream relays, $\boldsymbol{d} = 4$ is selected for *type II* relays. This allows *type II* relays to identify fault interruption operations by primary protection relays (*type I* relays) of zones 2, 3, 4 and 5 (lateral load feeders). Accordingly, the relay type is selected as given in Table 6. 3.

Table 6. 3 Relay type selection and protected zones of the DCMG network

Relay	**Relay type**	**Protected zone of the DCMG**
R_1	*Type II*	Primary protection – zone 1 Backup for- zones 2,3,4 and 5
R_2	*Type II*	Primary protection – zone 1 Backup for- zones 2,3,4 and 5
R_3	*Type II*	Primary protection – zone 1 Backup for- zones 2,3,4 and 5
R_4	*Type I*	Primary protection – zone 2
R_5	*Type I*	Primary protection – zone 3
R_6	*Type I*	Primary protection – zone 4
R_7	*Type I*	Primary protection – zone 5

The feature vectors are formulated by applying the time delays according to the selected embedding dimensions. The extracted feature vector is then fed into the classifier scheme for fault classification. The feature vectors $\boldsymbol{X^I}$ and $\boldsymbol{X^{II}}$ defined for two relays: *type I* ($\boldsymbol{d} = 2$) and *type II* ($\boldsymbol{d} = 4$) are represented by (6.8) and (6.9).

$$X^{I} = \begin{bmatrix} E_{1,t-1} & E_{1,t} \\ E_{2,t-1} & E_{2,t} \\ E_{3,t-1} & E_{3,t} \\ E_{4,t-1} & E_{4,t} \\ E_{5,t-1} & E_{5,t} \\ E_{6,t-1} & E_{6,t} \end{bmatrix} \quad \textbf{(6.8)}$$

$$X^{II} = \begin{bmatrix} E_{1,t-3} & E_{1,t-2} & E_{1,t-1} & E_{1,t} \\ E_{2,t-3} & E_{2,t-2} & E_{2,t-1} & E_{2,t} \\ E_{3,t-3} & E_{3,t-2} & E_{3,t-1} & E_{3,t} \\ E_{4,t-3} & E_{4,t-2} & E_{4,t-1} & E_{4,t} \\ E_{5,t-3} & E_{5,t-2} & E_{5,t-1} & E_{5,t} \\ E_{6,t-3} & E_{6,t-2} & E_{6,t-1} & E_{6,t} \end{bmatrix} \quad \textbf{(6.9)}$$

Where, $E_{1,t}$, $E_{2,t}$ …. $E_{6,t}$ are the RWE in the six decomposition levels of the t^{th} data window.

6.4.7. Feature vector comparison

To identify a general trend of RWE variation, 25 randomly selected events (using PSCD/EMTDC simulated data) under different fault/ non-fault cases are selected to extract the feature vectors shown in Figure 6.5;

a) ***DC side pole-ground fault***- RWE variation of decomposition levels at pole-ground fault events (set of 25 pole-ground faults simulated under different fault resistances, locations, incident times, etc.) is shown in Figure 6.5 (a). A general trend immerged shows that compared with non-fault events and pole-pole fault events there is a sudden increase of RWE in decomposition level 2 in all the time steps after a pole-ground fault. Set of 25 fault events selected represents a wide range of fault resistances and fault locations. Hence, it stands to reason that the trend of RWE distribution emerged is typical to the pole-ground faults in DCMGs.

b) ***DC side pole–pole fault***- RWE variation of feature vectors extracted during the occurrence of DC side pole-pole faults (set of 25 pole-pole fault events simulated under different fault resistances, locations, incident times, etc.) is shown in Figure 6. 5(b). The RWE variation clearly show an increase of RWE in decomposition levels 3 and 4 compared to during pole-ground fault events and other non-fault events. These characteristic

variations are visible in all 25 pole-pole fault events considered; hence, shows a characteristic trend to the pole-pole faults in DCMGs

c) ***Normal operation***- From Figure 6. 5(c), the energy activity of a healthy network under normal operation (simulated for different modes of operation under different loading conditions) is different from the faulted network. By comparison of RWE in different decomposition levels, fault events can be differentiated from normal operation of the DCMG.

d) ***Load switching***-During the load switching operation of a healthy network (25 load switch events selected during step changes to load by ±5%, ±10%, ±15%, ±20%, ±30%, ±40%), there is a sudden increase of RWE in decomposition levels 5 and 6 (see Figure 6. 5(d)), compared with other fault and non-fault events. This characteristic RWE variation allows load switching events to be distinguished from fault events.

e) ***Fault interruption in lateral feeders***- Upon detection of a fault in a lateral feeder(zones 2,3,4 and 5) by primary protection relay (relays R_4, R_5, R_6 and R_7), the faulted feeder is isolated by the DC circuit breakers at zones 2, 3, 4 and 5. The feature vectors are extracted from the current signal at the instance of pole-ground faults occurrence and immediate interruption (see Figure 6. 5 (e)). The trend of RWE variation indicates the occurrence of pole-ground faults in first two data windows (***t-3*** and ***t-2***) as the RWE in decomposition level 2 is more dominant, similar to during pole- ground fault events (see Figure 6. 5(a)). However, the energy variation in the decomposition levels of the next two data windows (***t-1*** and ***t***) indicates that the fault have been interrupted because the RWE in decomposition levels differs from that of pole-ground fault. This characteristic temporal variation of RWE within 4 time windows indicates that a pole-ground fault has occurred, and has been isolated by the primary protection of the faulted zone. Hence, the event is classified as a fault event in the network, but does not require the relays R_1, R_2 and R_3 to operate, since the faulted feeder is already isolated by the breakers.

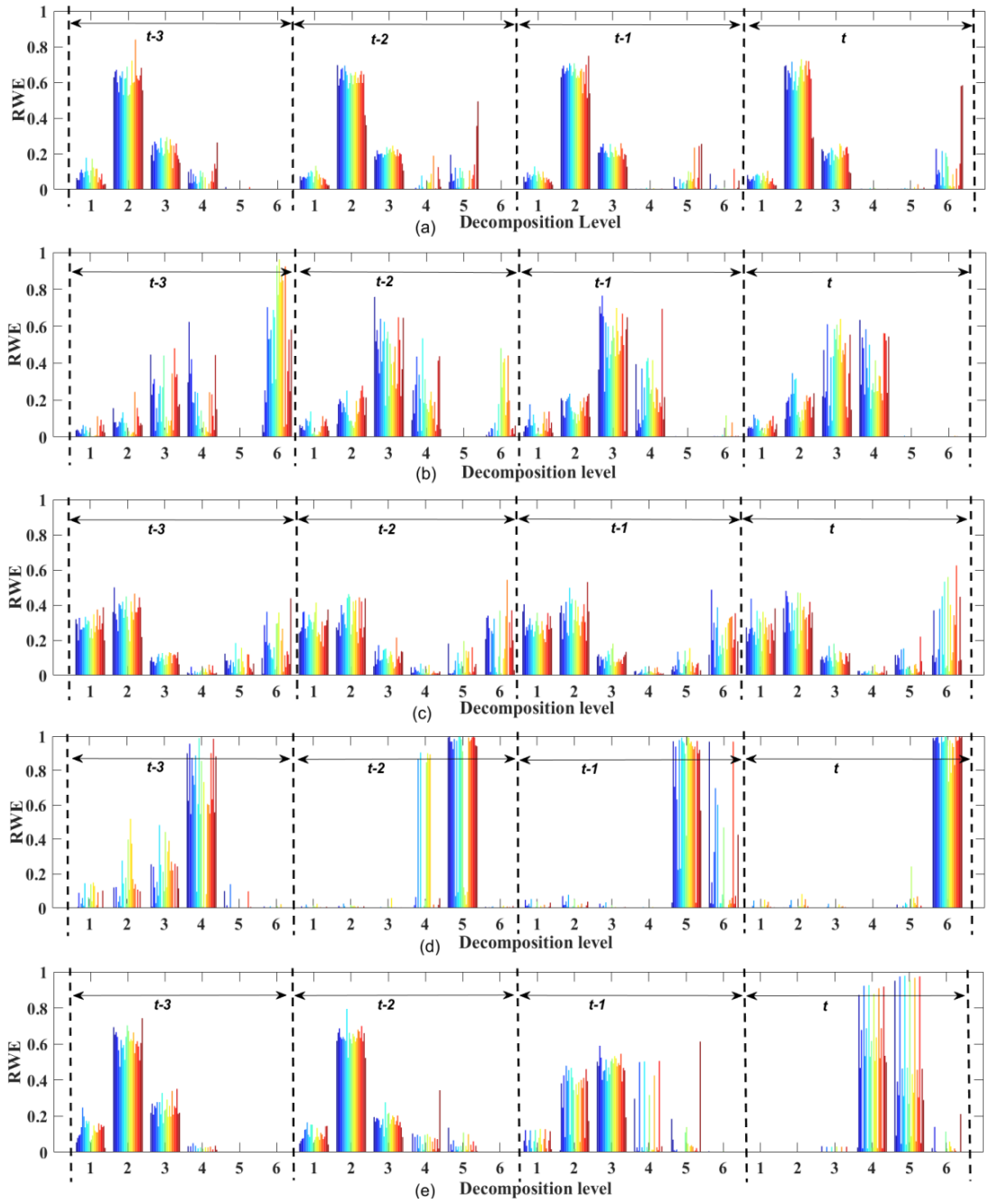

Figure 6. 5 RWE distribution diagram of the feature vector extracted from a) current signals during 25 pole- ground faults b) current signals during 25 pole-pole faults c) current signals during 25 normal operation conditions d) current signals during 25 load switch in-out operations e) current signals during 25 fault interruption operations by the primary protection relay of a lateral feeder.

Intermediate stages of signal processing (at relay R_1) from simulated current waveforms are shown in Figure 6.6 for a fault (DC bus pole- ground fault) and non-fault (load switching operation) event. The comparison shows how each signal

processing stage contributes in constructing the feature vector. This constructed feature vector is then fed into the ANN for fault detection and classification.

From the above comparison of RWE variation, it is clear that the ability of the proposed fault detection scheme to identify fault events can be realized by comparing the extracted feature vectors from line current signals. These extracted feature vectors are then used as inputs to the feed-forward ANN for training and event classification.

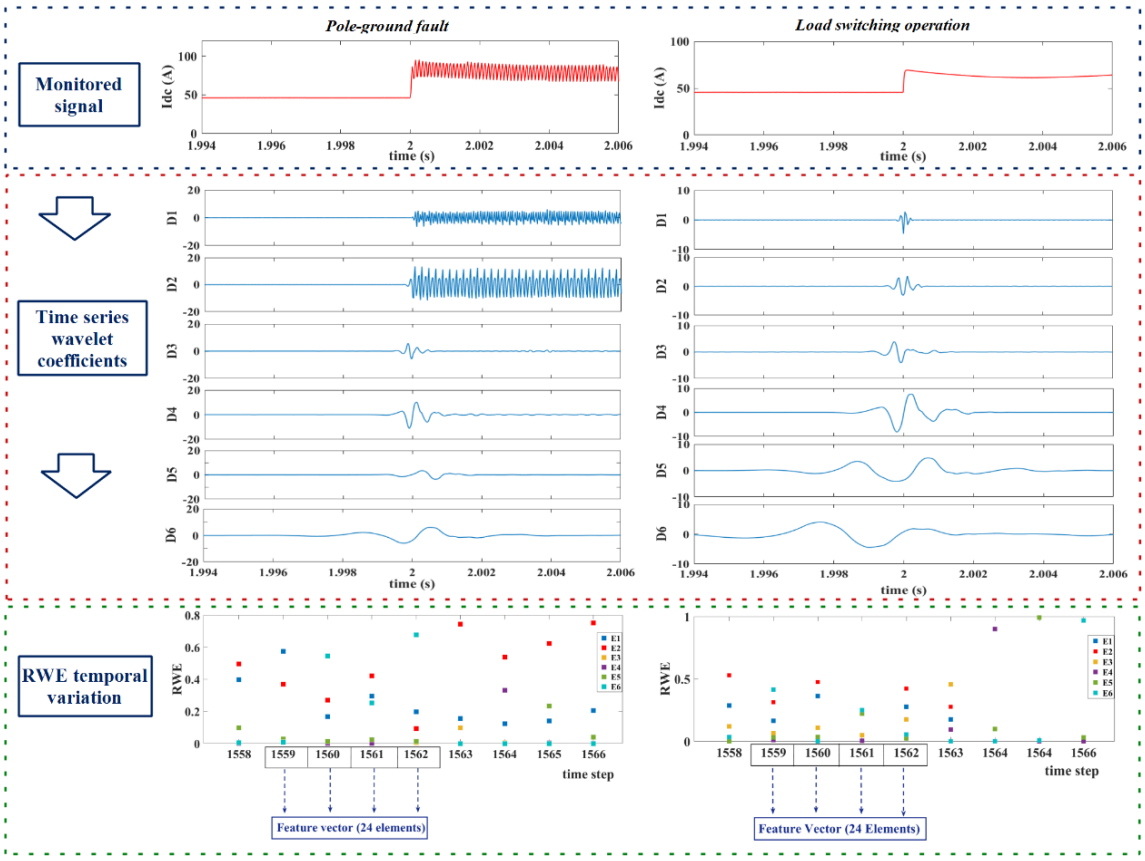

Figure 6. 6 Intermediary stages of signal processing of current with pole-ground fault (at t=2s), and load switching operation (at t=2s)

6.5 Fault classification

Recently machine-learning models are being employed extensively for classification, forecasting and clustering of data, in a vast field of applications. These machine-learning models are capable of achieving significant level of accuracy and calculation speeds, which makes them ideal for a wide range of engineering applications.

The process of developing a classifier for fault detection and localization involves deciding which feature to use for classification and which machine learning model achieves the best classification accuracy.

6.5.1. Classification methods

There are different classifier structures that could be employed for fault detection and classification. This study evaluated four different types of machine learning models on the basis of parameters such as classification accuracy, speed, model flexibility and memory usage.

1. ANN

ANN uses a soft criterion for feature comparison and has the ability to infer the underlying nonlinear and complex relationships between input and output data [154, 159, 162]. In the process of training the ANN, the training algorithm is presented with sets of input data and output labels. Through iterative training procedure, the ANN weights and biases are adjusted by error signal in a way that the network output tries to follow the desired output [162-166]. Figure 6.7 illustrates the basic structure of ANN as a classifier.

2. SVM

Support vector machines (SVM) is a linear classifier, which creates a line or hyperplane to separate data into classes. The SVMs can be used with both linear and non-linearly separable data. The aim of training the SVM is to maximize the margin between classes, and to minimize the over fitting of the classifier. Since not all data sets are linearly separable, kernel functions are used to transform linearly inseparable data to higher dimensional space in which they become separable. Linear, polynomial, radial or sigmoid functions can be used as the kernel function for mapping. Figure 6.8 illustrates the concept of SVM.

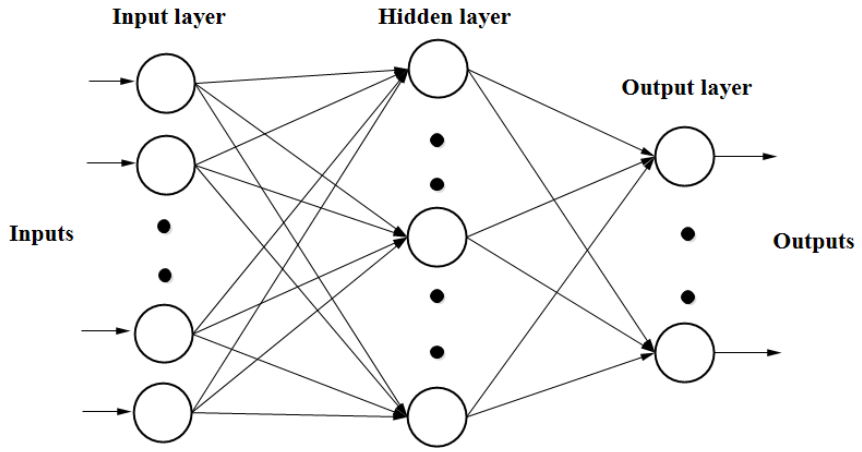

Figure 6. 7 Basic structure of ANN for classification

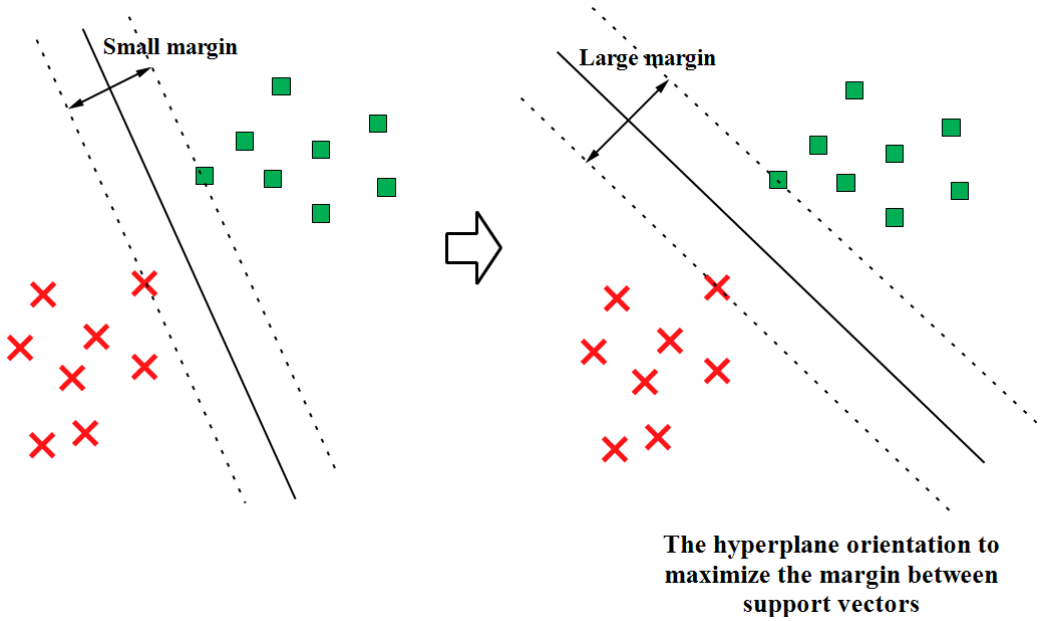

Figure 6. 8 Illustration of the concept of support vector machines

3. Decision trees

Similar to ANNs and SVMs, Decision trees are a classifier technique for mapping observations about an element to its target values. In the tree like structure, each internal node denotes a test on an attribute, each branch represents an outcome of the test, and each leaf node (terminal node) holds a class label. A decision tree learns from splitting training data into subsets based on test on an attribute. This partitioning is repeated recursively until a subset at a node has the same value of the target variable, or partitioning no longer adds value to the classifications.

4. K nearest neighbor (KNN)

KNN is a classification algorithm that stores all the training data and classifies the new data points based on a similarity measure how its neighbors are classified. In KNN, there is no explicit training phase before classification which means classification can be immediately started once the dataset is labeled. Major drawbacks of this classifier model are entire training data set need be kept in memory and is required to parse through all data points for each classification.

A comparison of different classifier models discussed above is provided in Table 6.4.

Table 6. 4 Comparison between classifier models.

Classifier model	Prediction accuracy	Prediction speed	Memory usage	Interpretability	Model flexibility
ANN	Medium/ High	Fast	Low	Low (black box model).	High
SVM	Medium/High	Depends on kernel type	Medium/ High	Depends on kernel type.	Depends on the kernel type.
Decision trees	Can have a low classification accuracy in certain cases.	Fast	low	High	Depends on the number of split settings.
KNN	High	Slow/ Medium	Medium/ High	Medium	Flexibility decreases with increasing number of neighbors.

6.5.2. Classifier selection

By comparing different classifier models, it could be concluded that the ANNs better suit this particular application, due to its high classification accuracy, fast classification times, low memory requirements and high flexibility compared with other classifier models.

6.5.3. Structure of the ANNS

Table 6.5 summarizes the learning parameters and structure of the two ANNs employed in the proposed fault detection and localization scheme. Trial and error approach was followed with feature vectors of different dimensions, the number of nodes in hidden layers and activation functions, and these parameters were selected to acquire the best classification performance. The structures of the two ANNs

selected manifest the best classification performance in terms of, classification accuracy and speed of detection.

Figure 6.9 (a) and (b) show the structure of ANNs used for fault detection and classification in a *type I* and *type II* relays respectively.

Table 6. 5 Architecture and learning parameters of ANNs employed for relay *type I* and *type II*

Architecture and learning parameters of ANNs	***Relay Type I***	**Relay *Type II***
Number of layers	2	2
Number of Neurons	Input layer:24 Hidden layer:20 Output layer:4	Input layer:12 Hidden layer:10 Output layer:3
Activation function	Tangent sigmoid	Tangent sigmoid
Learning rule	Levenberg–Marquardt Back-Propagation	Levenberg–Marquardt Back-Propagation
Mean squared error	1 e-5	1 e-5

6.5.4. ANN training

The backpropagation algorithm is used for supervised learning of ANN using gradient descent, to determine the weights and biases for the ANNs. In this technique gradient of the error function with the weights of the network is calculated. At the beginning, the gradient of the error function in the final layer of weights are calculated and then proceeds backward. Computations of the previous layer are used in the computation of the gradient of the next layer. This backward computation algorithm or the backpropagation algorithm facilitates the efficient calculation of the gradient at each layer. Thereby, adjusts the network parameters (weights and biases) to follow the expected behavior as defined by the labels at the training stage.

To train the learning parameters of ANN, sufficient previous knowledge that represents both fault and non-fault events is critical. Furthermore, the training data should include adequate information to carry out the tuning of these parameters approximating the expected behavior [165,166].

The data for ANN training comprised of fault current measurements and fault information can be obtained either from real time measured data or time-series simulated data. In this study, training data from PSCAD/EMTD time series simulations is used. The DCMG model discussed in Chapter 3 is used for to conduct

time-series simulations with different types of faults (i.e. pole-pole, pole-ground, arc faults), fault resistances, fault locations with varying network operating conditions and loading levels. In addition, non-fault events such as load switching operations and changes to the operating mode of the network were simulated under different conditions of operation. Different configurations for fault/non-fault simulations used are summarized in Table 6.6. In total, 5200 events (1800 fault and 3400 non-fault events) under different cases discussed above were simulated for ANN training and performance testing.

MATLAB code for trained neural networks for fault classification is provided in Appendix B.

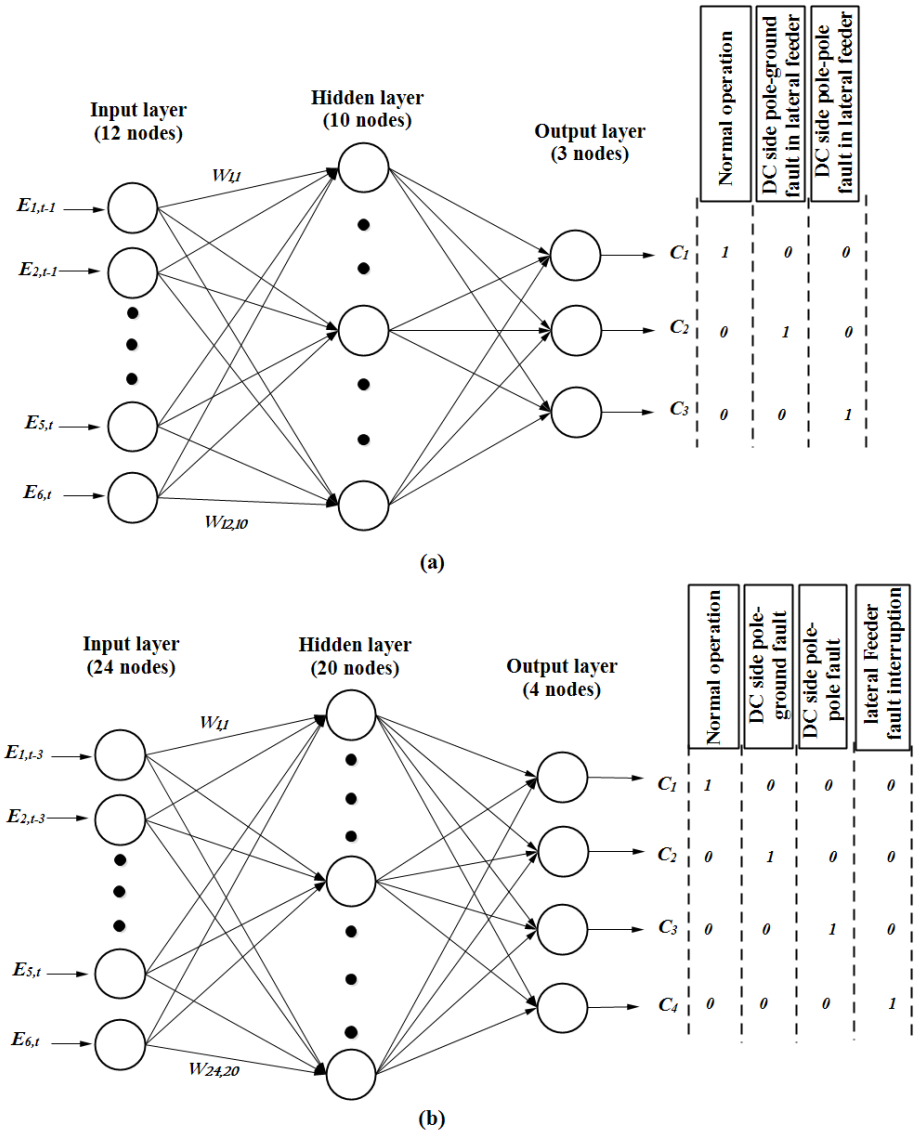

Figure 6. 9 structure of the employed ANNs for fault classification in a (a) *type I* relay, (b) *type II* relay.

Table 6. 6 Different configurations for fault and non-fault simulation in PSCAD/EMTDC

Variable parameter	**Configurations**
Fault type	DC pole- ground, DC pole-pole(both arc and non-arc faults)
Fault resistances	0.01Ω- 300Ω
Fault locations	DC bus, load feeders 1, 2, 3 and 4
Operating modes	Grid-connected, Islanded
Load feeder 1,2,3 and 4 – loading levels	Load feeder 1: 15kW – 0kW Load feeder 2: 25kW- 0kW Load feeder 3: 15kW-0kW Load feeder 4: 15kW- 0kW
Load switching	step changes to load feeder 1,2,3 and 4 by ±5%, ±10%, ±15%, ±20%, ±30%, ±40%
Fault interruption in load feeders	Faults interruption operations by the load feeder primary protection relays R_4, R_5, R_6 and R_7 due to; pole- ground faults and pole-pole faults in the load feeders (i. e protection zones 2,3, 4 and 5)

7. FAULT DETECTION AND LOCALIZATION PERFORMANCE

This chapter presents the evaluation of the proposed fault detection algorithm for its effectiveness in protecting DC networks. Fault detection and localization accuracy, fault detection time and robustness of the proposed scheme are considered in this regard. Furthermore, comparative analysis between the proposed technique and existing fault detection techniques is presented.

7.1. Classification accuracy

Fault detection and localization performance of the proposed scheme is evaluated using the classification accuracies calculated for each relay R_1 – R_7 for test data obtained using PCAD/EMTDC simulations. As explained in Section 6.5.4, training and testing data were obtained under different network configurations and fault parameters to provide the classifier with sufficient knowledge, which represents different operating conditions, to enable intelligent fault detection capability.

Figure 7.1 (a) - (g) shows the performance of the developed scheme using confusion matrices of the Relays R_1 to R_7 respectively.

In the confusion matrix, the output classes 1, 2, 3 and 4 indicate normal operation, pole-ground fault, pole-pole fault and fault interruption operation in lateral feeders, respectively. The events that were correctly classified are shown by the diagonal cells, and misclassified events are shown by the off-diagonal cells. The target class indicates the actual event while the output class represents the predicted event using the input feature vector. The column at the far right shows the classifier precision (how many classified events are correctly classified) of each relay in classifying an event. The row at the bottom of the plot shows the classifier sensitivity (how good at detecting a particular event) of each relay for a particular event. From Figure 7.1 (a) (confusion matrix of relay R_1) pole-ground fault is misclassified as a normal operational event, and a fault interruption operation in a lateral load feeder is misclassified as a ground fault in DC bus (zone 1) of the network (zone of the network protected by relay R_1. Overall classification accuracy of 99% is shown by relay R_1. The precision and sensitivity values of Relay R_1 for all output classes 1, 2, 3 and 4 are above 96%. Table 7.1 summarizes the sensitivity, precision and overall classification accuracy of each relay for the test data used.

Results reveal that each relay has the ability to achieve overall classification accuracy of higher than 98%. The test cases utilized for performance testing represent different configurations in the network; Hence, the test results show the intelligent fault detection capability unaffected by network operating conditions and different fault parameters. Furthermore, the sensitivity and precision of each relay for test cases obtained under different network events are more than 93%. Hence, the proposed scheme has a low false positive rate (high precision) while ensuring high sensitivity to network events, which reflect the accurate fault classification capability of the proposed scheme.

Figure 7. 1 Confusion matrix for test results obtained using test cases for relays (a) R_1, (b) R_2, (c) R_3, (d) R_4, (e) R_5, (f) R_6, (g) R_7.

Table 7. 1 Fault detection accuracies of the proposed scheme for the test data considered

Relay (*type*)	**No of test data sets**	**Sensitivity**				**Precision**				**Overall classification accuracy**
		Normal operation	Pole-Ground fault	Pole-pole fault	Fault interruption operation	Normal operation	Pole-Ground fault	Pole-pole fault	Fault interruption operation	
R1 *(type II)*	200	100%	96.2%	100%	97.7%	99.0%	96.2%	100%	100%	**99.0%**
R2 *(type II)*	180	98.8%	100%	96.8%	97.6%	98.8%	100%	93.8%	100%	**98.3%**
R3 *(type II)*	200	99.0%	100%	100%	97.7%	99%	96.3%	100%	100%	**99.0%**
R4 *(type I)*	180	99.1%	100%	97.4%	-	99.1%	100%	97.4%	-	**98.9%**
R5 *(type I)*	180	100%	97.3%	100%	-	99.1%	100%	100%	-	**99.4%**
R6 *(type I)*	180	99.1%	97.3%	100%	-	99.1%	100%	97.4%	-	**98.9%**
R7 *(type I)*	180	99.1%	100%	94.7%	-	98.2%	100%	97.3%	-	**98.3%**

7.2. Response time of the proposed schem

Sliding window time delay accounts for the highest share of fault detection time. In a *type I* relay, maximum sliding window time delay is: ($\boldsymbol{d}$ = 2) × (temporal window size = 1.28 ms) = 2.56 ms. In a *type II* relay, sliding window time delay is; ($\boldsymbol{d}$ = 4) × (temporal window size = 1.28 ms) = 5.12 ms.

DWT Mallat algorithm and ANN structure have a relatively low computational complexity; hence, low computational burden on CPU. The computational time of the developed algorithm is less than 50 μs, assuming all computations to be sequential (CPU clock speed of 100 MHz was considered in these calculations). Hence, the proposed scheme is capable of fault detection in a very short duration as explained below,

- Relays: *type I*- in less than 3 ms (sliding window time delay (= 2.56 ms) + computational time (< 50 μs))
- Relays: *type II*- in less than 5.5 ms (sliding window time delay (= 5.12 ms) + computational time (< 50 μs))

The above results show that the proposed scheme is very fast in terms of computational speed, thus supports the online implementation

7.3. Robustness of the proposed scheme

The monitored current signals can be degraded by the presence of noise. Furthermore, the DWT algorithm is not immune to noise. Hence, it is a major challenge when devising a transient based fault detection scheme.

Noise is the result of summing up a large number of independent parameters, and the sum of independent random variables is well approximated by Gaussian random variables. To evaluate the robustness of the proposing fault detection technique to the impacts of noise in the current measurements, white Gaussian noise of typical signal to noise ratio (SNR) values of 40 dB, 30 dB and 20 dB are added to the simulated current signals.

The features are extracted from noisy signals to construct the feature vectors which, is then used as the test data to evaluate the impact on overall classification accuracy by measurement noise. The performance of the relay R_1 under noisy current measurements is summarized in Table 7.2. The results show that the noise in the

measurements only has an insignificant impact on the classification accuracy of the proposed fault detection scheme. In the considered worst scenario of SNR = 20 dB, classification accuracy only decreases by 2% compared to that of current measurements without any noise. From the results, it can be concluded that the noise in the measured signal has only a trivial impact on the classification accuracy of the proposed fault detection technique.

The robustness of the proposed scheme is mainly down to the good generalization performance of the ANN classifier structure. However, employing noisy signals during the training of the ANN will reduce overfitting and have a regularization effect, which in turn could improve the robustness of the developed model. It recommended to carryout data augmentation by adding noise to signals to reduce the generalization error during the training.

Table 7. 2 Classification accuracy of relay R_1 with noisy current measurements

SNR	Overall classification accuracy
Without noise	99.0%
40 dB	98.5%
30 dB	98.0%
20 dB	97.0%

7.4. Comparison with existing schemes.

Table 7.3 provides a comparison of the proposed fault detection scheme with the existing DCMG fault detection schemes. From the comparison, the effectiveness of the proposed detection and localization scheme in terms of detection accuracy, fault detection speed, smart fault detection capability and robustness to noise is identifiable.

In addition to the effective fault detection, the proposed scheme is capable of successfully localize the faulted section of the network to isolate the fault quickly. The proposed scheme does not rely on communication and multi-terminal measurements for fault localization, unlike the fault detection schemes proposed previously.

Table 7. 3 Fault detection schemes for dc microgrids: comparison

Scheme	Fault localization & isolation capability	Communication requirements	Robustness to measurement uncertainty	Other remarks
Proposed scheme	Yes	No	Yes	• Overall fault classification accuracy of 98%-99%. • Intelligent fault detection capability with no communication. • Very fast selective fault isolation capability.
Overcurrent+ Rate of current rise+ change of voltage [20]	No	No	No	• Less sensitivity to high impedance ground faults • Issues may arise in protection coordination.
Overcurrent magnitude + direction of current [35]	Yes	Yes	Not mentioned	• Use communication between digital relays to locate the fault and isolate the faulted zone of the network
Overcurrent+ differential [22]	Yes	Yes	Not mentioned	• Use communication between digital relays to locate the fault and isolate the faulted zone of the network
Differential [19]	Yes	Yes	Not mentioned	• Rely on communication between protective relays on both sides of the protected zone for fault detection. • Drawbacks such as the inability to provide backup protection.
Wavelet transform [44]	Yes	Yes	Not mentioned	• common-mode currents at different network points are decomposed by applying WT to detect and localize ground faults
ANN [161,]	Yes	No	Not mentioned	• Directly use sampled current measurements for classification • Uses two neural networks for detection and location. • Complex classifier structure, hence leading to long training and detection times.

7.5. Concluding remarks

This chapter evaluated the performance of the fault detection and localization scheme proposed in this thesis. This scheme utilizes ANN as the classifier. It detects the fault conditions based on the extraction of fault features from the transient signals which occur during the fault.

The test results asserted that the proposed scheme has a 98% overall classification accuracy. The selected test cases represent a range of non-fault/fault events under different configurations. Hence, the test results reflect the capability of the proposed scheme to intelligently detect faults even under varying operating conditions.

The maximum fault detection time was calculated to be less than 5.5 ms, which shows the quick fault response capability of the proposed scheme. Furthermore, the proposed transient based fault detection scheme is robust to the impacts of signal noise.

Unlike most of the DCMG protection schemes discussed in the literature, the proposed scheme does not rely on communication between devices for fault localization. Hence, the proposed scheme does not require synchronized measurements and incur additional costs for setting up a communication network. Compared with currently available fault detection techniques, the proposed scheme showed better performance in terms of classification accuracy, fast response time, fault localizing capability and robustness to disturbances.

8. CONCLUSIONS AND CONTRIBUTIONS

This chapter presents the conclusions and summarizes the main contributions of the study. In addition, it proposes directions for future research in the area of DC network protection.

8.1. Conclusions

This thesis investigated on protection and grounding of DC microgrid networks. Initially, the focus of this research study was to identify the transient fault characteristics of DC microgrid networks. DC microgrid fault responses under pole-ground and pole-pole faults were investigated to identify the protection requirements.

Different grounding configurations for DC microgrid grounding were investigated considering ground fault current limiting capability, fault ride-through capability, ability to detect ground faults reliably and minimizing stray current. A reliable grounding strategy was developed, based on the application the DC microgrid network is being used for.

The thesis proposed a multi-resolution analysis based classification scheme for reliable detection of DC microgrid faults. Fast and accurate fault classification capability of the proposed scheme was discussed in the performance analysis.

The major conclusions drawn from this study are:

Unlike AC networks, the need for fast detection and localization were identified as the main protection challenges associated with DC networks. Also, the requirement of reliable protection coordination scheme that could facilitate selective fault isolation capability was also identified through the literature review.

The DC microgrid network model was developed in PSCAD/EMTDC for simulation studies. The DC microgrid model includes grid-connected VSC, solar PV plant and battery storage to supply network loads. DC bus voltage signaling based distributed control scheme was adopted in modeling the network. The ability of the developed network model to maintain DC bus voltage stability under different operating conditions and events was investigated. Currently, the standard for the design and operation of DC microgrids are not available. However, the simulation results have shown the capability of the modeled network to adhere to the basic control requirements.

Determinant factors in designing a DC microgrid network grounding scheme were identified in this thesis. Different tradeoffs are taken into consideration when deciding a grounding configuration for a DC network. Certain applications require a reliable supply of power unaffected by fault conditions. Hence, it requires the network to ride-through ground fault situations. High resistance grounded networks facilitate fault ride-through capability, are prone to transient over-voltages and voltage fluctuations. Conversely, DC networks for domestic applications require the ground fault to be detected quickly to ensure the safety of the personnel. Accordingly, a wide system study is required in selecting the DC microgrid grounding configurations. The selection of ground fault detection technique is based on the employed grounding configuration.

Fault responses of the DC network under different fault events were investigated. Fast capacitor discharge and the current rise in DC systems impose strict time limits for fault interruption. Furthermore, the absence of frequency and phasor information makes the fault localization more challenging. Hence, the use of conventional detection schemes is not straightforward. To provide a protection solution, wavelet – ANN based fault classification was proposed. The scientific hypothesis behind the new fault detection technique is "transient fault response of the DC microgrid network contains unique signatures that allow identifying the occurrence of the fault event," which was proved through results. A methodology for feature extraction using DWT analysis was developed. The extracted feature vectors from the training data were utilized to train an ANN, which was used as the classifier model. The use of ANN as the classifier model adds smartness to the developed algorithm. It enabled reliable fault detection unaffected by fault resistance, fault location, the operating mode of the network, loading conditions and other network events in the network.

The developed fault classifier scheme showed an overall classification accuracy of above 98% when tested with test data for its performance. The fault detection time was calculated to be less than 5.5 ms under all the cases tested. The proposed algorithm has a very low computational burden due to fewer input data and computationally efficient nature of WT and ANN algorithms. It was also found to be robust to the impact of noisy signal measurement. Under the worst case scenario of

20 dB considered in the study, the overall classification accuracy decreased only by 2%.

Conventional DC network fault protection schemes rely on communication to achieve proper coordination and selective fault isolation capability. In contrast, the proposed scheme is capable of isolating the faulted feeders and maintaining coordination between relays by time grading of the relay. Furthermore, the proposed scheme has the ability to provide backup protection to selected DC network zones.

As the fault detection is carried out by using ANN, the ANN needs to be retrained whenever there is a major change to the network, such as change of the network configuration, grounding configuration or addition of new DGs to the network.

In terms of reliability, detection accuracy and selectivity the proposed multi-resolution analysis based classifier scheme showed a better performance when compared with other DC network protection schemes. The ability of the proposed scheme to provide intelligent fault protection regardless of changes to the operating condition of the network stands out.

8.2. Contributions

The main contributions of this thesis are listed below:

1) Design and modeling of a notional DC microgrid model on simulation platform and evaluation of the operational performance of the DC microgrid model using a case study. In addition to the study on the protection of DC microgrids, this DC microgrid model can be employed for further studies on control and operation, islanding detection and power quality.
2) Investigation of fault response of the DGs and power electronic converters connected to the DC microgrid network was carried out. Transient and steady state performance of the network under different faults and effects of fault parameters on fault current was discussed. These fault characteristics exert an important influence in the design of fault detection techniques, relay coordination and fault interruption schemes.
3) Investigation of different DC microgrid grounding schemes for safe and reliable operation of the network. In this microgrid, several grounding

configurations were evaluated based on their ability to provide adequate ground fault protection, facilitate fault detection, ability to continue without immediate shutdown and immunity to transient over-voltages and voltage fluctuations. Based on the findings, an application based grounding strategy was developed, which could be adhered to when designing a DC microgrid network.

4) Demonstration of the applicability of the transient based fault detection technique for DC networks. The results show that the characteristic fault features can be extracted and be used for training a classifier for fault classification.
5) Confirmation of the effectiveness of the multi-resolution analysis-classifier based fault detection scheme to detect DC microgrid faults in a timely and accurate manner.

Journal papers

i) D. K. J. S. Jayamaha, N. W. A. Lidula and A. D. Rajapakse, “Protection and Grounding Methods in DC Microgrids: Comprehensive Review and Analysis”, Renewable and Sustainable Energy Reviews, vol. 120, p. 109631, 2020.
ii) D. K. J. S. Jayamaha, N. W. A. Lidula and A. D. Rajapakse, "Wavelet-Multi Resolution Analysis Based ANN Architecture for Fault Detection and Localization in DC Microgrids," in IEEE Access, vol. 7, pp. 145371-145384, 2019.

Conference papers

i) D. K. J. S. Jayamaha, N. W. A. Lidula and A. D. Rajapakse, "Wavelet Based Artificial Neural Networks for Detection and Classification of DC Microgrid Faults," 2019 IEEE Power & Energy Society General Meeting (PESGM), Atlanta, GA, USA, 2019, pp. 1-5.
ii) D. K. J. S. Jayamaha, N. W. A. Lidula and A. D. Rajapakse, "Bus Voltage Signalling Based Coordinated Control of DC Microgrids," 2018 Australasian Universities Power Engineering Conference (AUPEC), Auckland, New Zealand, 2018, pp. 1-6.

iii) D. K. J. S. Jayamaha, N. W. A. Lidula and A. D. Rajapakse, "Ground Fault Analysis and Grounding Design Considerations in DC Microgrids," 2018 IEEE 4th Southern Power Electronics Conference (SPEC), Singapore, Singapore, 2018, pp. 1-8.

8.3. Suggestions for future research

The hypothesis that the transients generated during DC network faults contain features that allows the identification of the fault was proved in this thesis. The test results showed the effective performance of the proposed algorithm.

The weaknesses of the proposed fault classification were identified. The ANN classifier is required to be trained separately for each microgrid. Considering the fact that transient behavior of DC microgrid network shows the same pattern irrespective of number of generators and network configurations. Further research in this area could lead to a more generalized fault detection scheme for DC microgrids.

The thesis results were entirely based on simulation studies. Verifying these research findings on a real DC microgrid test system is an essential step towards practical implementation.

Use of fault current blocking converter for DC fault current interruption is an under researched topic. Coordinated control of fault blocking converters and breakers can facilitate quick fault isolation, minimize damages to the network and minimize interruptions. Further investigation on DC breaker and fault blocking converter technologies is required.

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Appendix A

MATLAB code for DWT decomposition and RWE calculation

```
function output1=relative_energy1(x,interval,levels)

%x is 1 dimensional signal of column vector
%interval must be the number of k*(2^levels),where k is an integer.
% levels is the number of level for wavelet transformation(WT)

[c,l]=wavedec(x,levels,'db5'
y= sum_rela1(c,l,interval);
output1=relative_energy1(y);

plot(output1');
title('relative wavelet energy');
legend('p1','p2','p3','p4','p5','p6','p7','p8','p9','p10','p11','p12
');%This should be corresponding to the levels you defined.


function y=relative_energy(DATA)

           [M,N]=size(DATA);
          y=zeros(M,N);

           relative=sum(DATA);
          for n=1:N
              for m=1:M
                  y(m,n)=DATA(m,n)/relative(n);

              end
          end


function y=sumup1(DATA,interval)
    [M,N]=size(DATA);
   N1=floor(N/interval);
     y=zeros(M,N1);

  for k=1:M
        for l=1:N1
            m=0;
            for n=1:interval
                m=DATA(k,(l-1)*interval+n)+m;
            end
           y(k,l)=m ;
        end
  end


function [yout]=sum_rela1(c,l,N1)

        c=c.*c;
         N2=length(l)-2;
         a=zeros(N2,l(N2-1));

         for k=1:N2
             a(k,(1:l(1+k)))=c((sum(l(1:k))+1):sum(l(1:(k+1))));
         end
         N3=N1/2^(N2);
```

```
          N4=floor(l(2)/N3);
            b=zeros(N2,N4);

            for k=1:N2
                k1=log2(N3)+k-1;
                x=sumup1(a(k,:),2^k1);
                b(k, 1:(ceil(l(k+1)/2^k1))-1)
=x(1:(ceil(l(k+1)/2^k1))-1);
            end
            z=b;
            for s=1:N2;
            z(s,:)=b(N2+1-s,:);
            end
            y=z(:,1:(ceil(l(k+1)/2^k1)-1));
            yout=relative_energy1(y);
```

Appendix B

MATLAB code for trained neural network (for relay *type I*)

```
function [y1] = myNeuralNetworkFunction5(x1)
%MYNEURALNETWORKFUNCTION neural network simulation function.
%
% Generated by Neural Network Toolbox function genFunction, 16-Jul-
2019 12:41:11.
%
% [y1] = myNeuralNetworkFunction(x1) takes these arguments:
%   x = 12xQ matrix, input #1
% and returns:
%   y = 3xQ matrix, output #1
% where Q is the number of samples.

%#ok<*RPMT0>

% ===== NEURAL NETWORK CONSTANTS =====

% Input 1
x1_step1.xoffset = [7.41713745584013e-07;1.24452957589324e-
06;0.000228019871979377;3.12984370740438e-07;1.03390398424087e-
08;1.66345671238199e-10;1.13514242063214e-06;1.18093281501771e-
06;4.60300976112094e-07;8.09972903379445e-06;6.56725099569874e-
05;9.28135990731856e-08];
x1_step1.gain =
[3.36836139750438;2.27359774391729;3.08063187633531;2.01949217774794
;12.0222523896337;2.07778555529724;3.305218404499;2.82739007840941;2
.63460147071259;2.01872582769717;2.00211719860811;3.19250643208893];
x1_step1.ymin = -1;

% Layer 1
b1 = [-1.3670780901326223;-
1.3870600439480978;0.58270345507126164;0.18087606933975744;0.2049468
069078747;0.10591295757653856;-0.5787321800590377;-
0.74960571460253989;1.2278292329188398;-1.6184615665451172];
IW1_1 = [-0.21422726083112736 -0.087172183956076274 -
0.089710694904352045 0.03903486776259131 -0.958222091098894
0.80182214124255324 -0.32180635392530071 -0.77876929979241116
0.91381614005062595 -0.63174808260293047 -1.2516223949680938
0.41904316514558182;0.53898049569143758 -0.032446377809270385
0.41012718294054273 -0.74211436695737887 -0.74561902989224726
0.29382076044021166 0.0044831322515047709 0.55154873685217598
0.12477572284996213 0.26351971190012252 0.39770287375263169
0.77189434813128177;0.27688483108566064 0.36257103903397564 -
0.12847084266622835 -0.039875153860749343 0.71195954081085822
0.29133731506921495 0.88487013336351583 -1.0140656284363201 -
1.1253070358915893 -0.098367182633814637 0.42993142085073571 -
0.2452471083780626;-1.639977030464034 0.1324875517489203
0.94725191970038536 0.46594702746401184 -0.058342263886751851
0.76887165695313053 -1.2124429861914159 0.45842540719188801
0.28397043990982235 -0.83627673692434945 0.55125848536813671 -
0.20070861125745623;-1.1347167198363823 2.4895434353755199 -
0.2903548158783959 0.27951371555847276 -0.18428919608028282
0.23566402026501707 -0.82153636923871443 0.82332666039298497
0.76689716482375403 0.19783173217512215 0.41323370853145863 -
0.11985619896516497;0.1124101920612972 -0.32919821178467379 -
0.82441777938206207 0.52346577845805131 -0.19393262904340242
1.0371119357319618 1.087371884547087 0.017990454323957569 -
```

```
0.23578965344920866 -0.91474214669173037 -0.21349830151350088
0.25326798691021951;-0.90633156133661896 -1.0499980015212611
0.90139712870843747 0.17783674995553342 -0.8372957757771029
0.46096315181139752 -0.10369097862998716 0.37565137503372703
1.7822228615247278 -0.13105593854995737 -1.3190837195937331
0.3880837467930745;-0.92378145569887937 0.05962294654531039
0.32256444761584158 -0.54674533000162229 -0.78680280041457351
0.52699532853055431 0.21233376886365238 1.1046147254463288 -
0.10688193608490937 -0.64308050061254041 -0.64920337689945284 -
0.55977790294343643;0.28318106446196206 2.0504922468042501 -
0.60643040577885832 0.011890095160058858 0.84517873573956259 -
0.38188141975537859 0.17720856431847837 1.1093867954907919 -
0.59266664262518298 -0.72716540288802811 0.30490272672263374
0.15066270765361228;-0.29098109577532133 0.64834324760352402
0.63499413589517828 -0.65652988541668722 0.0015067757599291024
0.80986075826825032 -0.051903380269164842 -0.026628073096886092
0.27888910077100026 -0.48020225653145915 -0.039496453511118607 -
0.74096581087588598];

% Layer 2
b2 = [0.10054324894120217;-0.37320428030800545;-1.0310483149862089];
LW2_1 = [-1.6775808280050302 -0.14126720769930776 1.6888133679051447
-1.4860752411644791 -1.2478841264335592 0.50772099133732207 -
2.3238141006265023 -1.337536053728946 -0.36884604594369397
0.10366129849998276;-1.2463479466898864 0.32702541644233901
0.21472304317978416 1.4685403255521998 3.0533149134611151 -
1.324759425755315 -0.46796151909598205 -0.20962098792612266
1.9377215376341865 0.76893598721863421;0.75235075341919644 -
0.69226561061827907 -0.10812697091670655 0.73403528099680637
0.45236144935218031 -0.0038228139234408672 1.9997006313274257
0.40670940345091616 -2.2878859417144013 0.638080927644328221;

% ===== SIMULATION ========

% Dimensions
Q = size(x1,2); % samples

% Input 1
xp1 = mapminmax_apply(x1,x1_step1);

% Layer 1
a1 = tansig_apply(repmat(b1,1,Q) + IW1_1*xp1);

% Layer 2
a2 = softmax_apply(repmat(b2,1,Q) + LW2_1*a1);

% Output 1
y1 = a2;
end

% ===== MODULE FUNCTIONS ========

% Map Minimum and Maximum Input Processing Function
function y = mapminmax_apply(x,settings)
y = bsxfun(@minus,x,settings.xoffset);
y = bsxfun(@times,y,settings.gain);
y = bsxfun(@plus,y,settings.ymin);
end

% Competitive Soft Transfer Function
function a = softmax_apply(n,~)
```

```
if isa(n,'gpuArray')
    a = iSoftmaxApplyGPU(n);
else
    a = iSoftmaxApplyCPU(n);
end
end
function a = iSoftmaxApplyCPU(n)
nmax = max(n,[],1);
n = bsxfun(@minus,n,nmax);
numerator = exp(n);
denominator = sum(numerator,1);
denominator(denominator == 0) = 1;
a = bsxfun(@rdivide,numerator,denominator);
end
function a = iSoftmaxApplyGPU(n)
nmax = max(n,[],1);
numerator = arrayfun(@iSoftmaxApplyGPUHelper1,n,nmax);
denominator = sum(numerator,1);
a = arrayfun(@iSoftmaxApplyGPUHelper2,numerator,denominator);
end
function numerator = iSoftmaxApplyGPUHelper1(n,nmax)
numerator = exp(n - nmax);
end
function a = iSoftmaxApplyGPUHelper2(numerator,denominator)
if (denominator == 0)
    a = numerator;
else
    a = numerator ./ denominator;
end
end

% Sigmoid Symmetric Transfer Function
function a = tansig_apply(n,~)
a = 2 ./ (1 + exp(-2*n)) - 1;
end
```

MATLAB code for trained neural network (for relay *type II*)

```
function [y1] = myNeuralNetworkFunction(x1)
%MYNEURALNETWORKFUNCTION neural network simulation function.
%
% Generated by Neural Network Toolbox function genFunction, 13-Jul-
2019 14:36:45.
%
% [y1] = myNeuralNetworkFunction(x1) takes these arguments:
%   x = 24xQ matrix, input #1
% and returns:
%   y = 4xQ matrix, output #1
% where Q is the number of samples.

%#ok<*RPMT0>

% ===== NEURAL NETWORK CONSTANTS =====

% Input 1
```

```
x1_step1.xoffset = [7.41713745584013e-07;1.24452957589324e-
06;2.05404144626562e-06;3.41871732022462e-08;1.03390398424087e-
08;1.66345671238199e-10;1.13514242063214e-06;1.18093281501771e-
06;4.60300976112094e-07;8.09972903379445e-06;4.11993024127739e-
06;7.06489993188392e-10;2.47976033275097e-08;1.51601977770661e-
06;6.27786774488512e-07;2.33599051477167e-07;3.33609721318733e-
07;5.67923086079144e-10;0;0;0;0;0;0];
x1_step1.gain =
[3.36836139750438;2.18680623366007;3.07956000846585;2.01949160923202
;13.1100075194219;2.15246878546083;3.31381015632431;2.33759916496653
;2.63460147071259;2.01878663372287;2.00199384027371;3.19250596270669
;2.91324079714225;2.30252080501727;2.61318591873236;2.68765429698882
;2.00028792436518;2.00034939958577;3.2108581049733;2.75779318824971;
2.76637685027013;2.01565936575002;2.04352487206712;2.00013626861272]
;
x1_step1.ymin = -1;

% Layer 1
b1 = [1.1711694891243225;1.4101386907927564;1.3703793811789136;-
0.94361580794947464;-0.9592240042344311;0.89166902794140601;-
0.51997781553970079;-0.41151420493837948;-0.17227333979192197;-
0.109019914358523;-
0.10794466294880713;0.12189865773198692;0.40828249166360125;0.514678
03445568616;0.54171904288686812;1.0019350281879791;-
1.5062470389701659;-1.1411432959521908;-1.3758824431072449;-
1.292213191672551];
IW1_1 = [-1.5534059730512075 3.0660563972017818 -1.0475822124240521
0.25833734279276704 0.25100402823972834 -0.39633862805646947 -
0.04195375563392871 1.3724595176306136 0.50107619220531208 -
0.27453311482780607 0.3096033704799766 -0.48876969816014521 -
0.77144215360749746 0.62247868668957695 0.80654238530447875
0.44329307568764537 0.85975865155122555 -0.38488233216842532 -
0.26979299219586916 0.75310009494197483 0.5728931920622975
0.33913064491182759 0.39550044226894898 0.61263310238251412;-
0.38509900186324691 -0.010087769468645345 0.48573792186389059
0.22715999756926036 -0.19303576499695038 0.051410114080564936
0.28544867811201108 0.65226350922353227 -0.5202767504244028 -
0.36909649606202888 0.29639159009266558 -0.48311065368809758
0.23352551929086762 -0.029207176617318545 -0.13812332993631221
0.35313664580528997 0.42258637148524564 0.38227604897678302
0.26198804624167521 -0.40713799225653791 0.12392539167618265
0.34094522372287811 0.0067662210370666009 -
0.18744153969324528;0.70523982726029266 -1.2385559791444074
0.35459764446840958 -0.10312888610448556 0.025019294249821578 -
0.249628408071846 0.66882540319173633 0.59757975771320426 -
0.81207258550754691 0.36055073204839932 0.102032728626008
0.64160437208264431 0.70858108410858989 -0.22353414587612663 -
0.14157014074893109 -0.88998228107273381 -0.061732963464424237
0.91815455138651469 0.52884002161774379 -1.2238947548639936 -
1.2884867988109716 0.48160097784951533 0.95059736611474133 -
0.25907168145554521;0.23358732883274785 -0.649247080251525 -
0.031082623357121204 -0.34947994413820854 -0.5696894040677748
0.016415166260224812 -0.50603113869227412 -0.77315802675653877 -
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0.47431253891943859 0.36292784780521042 0.03842684749104569
0.068930650546248584 0.42518581624860929 0.29735134805797436
0.16098435762440172 -0.29412293902698222 -0.46577636355289798
0.34383372717006971;0.28368536885418516 0.01262054512378331
0.11523778240199226 -0.048809063578347217 -0.19180690860947705
0.26644172892938489 -0.46202684454227216 -0.13873141295806291
```

0.038644207460160042 0.60430484009247754 -0.7322703514073996
0.12312246557278612 0.2721509651536157 0.44536989786168057
0.58604418812105075 0.40954106305769028 0.6293084085280124 -
0.34727291232484186 -0.10511476404845485 -0.21411141865838473 -
0.44374507619300047 -0.16709076467724826 -0.23241516776266111
0.1757435806555423;-0.49857403339535955 0.11723207641782041
0.21975067968174902 -0.32693532480758392 -0.55212389245023696
0.10981007668587908 -0.48355061220218398 -0.21653200654815682 -
0.58886104201072287 -0.22893224016618571 0.052003579865982544 -
0.28416372418455893 -0.24889454653532747 -0.09715933947543573 -
0.075489949443000359 -0.048966820708655406 -0.14147174272150 52
0.42282236291666858 0.1120823299954519 0.39470480018974535 -
0.34903761118426707 -0.56844042286676499 0.25288886379654574 -
0.49650228485239245;1.1626970492622939 -0.98533446737406849
0.49273167562402315 -0.47831997271893362 0.49204063432474604
0.066645080860361874 0.64705734375537316 -0.22180127541406172 -
0.65309347632498627 -0.2405740133931141 -0.18377186371510115 -
0.15876603728097208 0.29544981259245229 -0.73732014468940099 -
0.32796809989704795 -0.4837195579369255 -0.10773275041416586
0.037473101330950817 0.34366839834272039 -0.40493560929207678 -
0.6902962672826406 -0.39437355667446505 0.73214532232850948
0.46414388489686792;0.10704160981387252 0.58142259835920951 -
0.48768165332174007 -0.33286553874617525 0.16798124932553241 -
0.26092334866173755 0.28297517225603536 0.26056196030738732 -
0.3041855170781117 -0.4804823537844809 -0.43183997098979326
0.041915248912231556 0.17398663883676985 0.3169287300546505 -
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0.35818366695121723 -0.19509531295474314 -0.25391432480722637
0.022729781321289888 0.66924541384407876 0.50191177075339199 -
0.53218653245117453;0.26087900005063669 0.99798722069375079 -
0.71565167826634035 0.049155021380503545 0.12852517570520383 -
0.18154984312689884 0.2296997996274116 0.79322034897879379 -
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0.059178502228751782 -0.16764735154173502 -0.54602519323879573 -
0.31474179831144078 0.40639873768609752 -0.15647638402668215 -
0.22364924554432994 0.27246732941461332 0.38665836939878317
0.54074547172110965 0.24166748662919282 0.27853388719153632
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0.26441217542014922 -0.48930189296328985 -0.046819039993358923

```
0.14464472760521957 0.036423753152893687 0.088270439517067478 -
0.63591786768015213 -0.45400374488709888 0.003626673709455601
0.21258949473849417 -0.49430157257055413 -0.54840984300367379
0.041744488077461506];

% Layer 2
b2 = [-0.58699201021205027;-
0.46426918289001395;0.445201886538308;0.4469058693712411];
LW2_1 = [-3.1811206237962386 0.10804647752471187 2.5931651323027016
0.48615333845440395 0.62985181782629951 1.1840861752224519
1.8131034861690056 -0.2361384829013605 -0.58426872588896894 -
1.0844545154780707 0.695430256671834 -1.8755585282421297 -
0.37321787459817152 -0.65015402544929202 -0.78598948919607481
1.0089093878394009 -2.9970977344192304 -0.30141601196064394
1.3319733693172651 0.33866133802305814;2.8999498831309443
0.39499846572693292 -1.5762671476665162 0.17212557967683514 -
0.26245082586626489 -0.4389362561607042 -1.6106414238693476 -
0.77757849868516216 0.68518319433205921 -0.15464295666478764
0.67409381513005595 -1.5937559394208112 -0.92504828923400684
1.5443617945904127 1.033603150832666 -0.1499878502113878
3.4949126973794997 -0.87795402101485864 0.84144647126420224 -
0.79253134048109686;-0.57685711538441165 0.0034856369608933422 -
0.67503301359618639 0.17882837552221728 0.14514856268326987
0.65238120333538774 -0.2051352900112296 0.21644719672477328 -
1.4436967707371204 0.79658585372102819 -1.6548437417340112
1.0086468244941871 1.9575441552358994 -1.6218269011634343
0.83292391604749338 1.3601255233940854 -0.2337972870896082 -
0.30667862597194367 -1.9198047894626475
1.0168859259112422;1.127377094244062 0.74893713113639193
1.0362783432252356 -1.1174267560433162 0.20244770477626109
0.35719738945322443 0.013913040418190413 0.49244197414058616
0.63755450400579894 0.96945738397811643 0.25940806815525758
2.2601225356643648 -0.21214666975669547 1.5840790829623215 -
0.84477922919053094 -2.5956293834617488 -0.38149262777556586 -
0.41035803527886466 -2.346484319859834 0.0519681624582686 92];

% ===== SIMULATION ========

% Dimensions
Q = size(x1,2); % samples

% Input 1
xp1 = mapminmax_apply(x1,x1_step1);

% Layer 1
a1 = tansig_apply(repmat(b1,1,Q) + IW1_1*xp1);

% Layer 2
a2 = softmax_apply(repmat(b2,1,Q) + LW2_1*a1);

% Output 1
y1 = a2;
end

% ===== MODULE FUNCTIONS ========

% Map Minimum and Maximum Input Processing Function
function y = mapminmax_apply(x,settings)
y = bsxfun(@minus,x,settings.xoffset);
y = bsxfun(@times,y,settings.gain);
y = bsxfun(@plus,y,settings.ymin);
```

```
end

% Competitive Soft Transfer Function
function a = softmax_apply(n,~)
if isa(n,'gpuArray')
    a = iSoftmaxApplyGPU(n);
else
    a = iSoftmaxApplyCPU(n);
end
end
function a = iSoftmaxApplyCPU(n)
nmax = max(n,[],1);
n = bsxfun(@minus,n,nmax);
numerator = exp(n);
denominator = sum(numerator,1);
denominator(denominator == 0) = 1;
a = bsxfun(@rdivide,numerator,denominator);
end
function a = iSoftmaxApplyGPU(n)
nmax = max(n,[],1);
numerator = arrayfun(@iSoftmaxApplyGPUHelper1,n,nmax);
denominator = sum(numerator,1);
a = arrayfun(@iSoftmaxApplyGPUHelper2,numerator,denominator);
end
function numerator = iSoftmaxApplyGPUHelper1(n,nmax)
numerator = exp(n - nmax);
end
function a = iSoftmaxApplyGPUHelper2(numerator,denominator)
if (denominator == 0)
    a = numerator;
else
    a = numerator ./ denominator;
end
end

% Sigmoid Symmetric Transfer Function
function a = tansig_apply(n,~)
a = 2 ./ (1 + exp(-2*n)) - 1;
end
```