References

- [1] Wenxin Wang, Study of "Low Power Multi-threshold CMOS circuit optimization and CAD design", The University of Guelph, May. 2004
- [2] Paulo Francisco Butzen, and Renato Perez Ribas, "Leakage Current in sub-micrometer CMOS gates", Universidade Federal do Rio Grande do Su
- [3] Ajith Pal, "Lecture 26: Power Disipation in CMOS Circuits", Department of Electrical Engineering, IIT Kanpur, India
- [4] Amit Singh Gaur, and Jyoti Budakoti, "Advanced Low Power CMOS Design to reduce power consumption in Deep Submicron Technologies in CMOS Circuit for VLSI Design", International Journal of Advanced Research in Computer and Communication Engineering, Vol. 3, Issue 6, June 2014
- [5] Nandita Dasgupta, "Lecture 1 Introduction on VLSI Design", Department of Electrical Engineering, IIT Madras, Jan 2009
- [6] Sheu, B. J. et al. "BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors", IEEE Journal of Solid State Circuits, New York, v.SC-22, n.4, p. 558-566, Aug. 1987
- [7] R. Saleh, "Lecture 6 Leakage and Low-Power Design", Dept. of ECE University of British Columbia
- [8] Chris H. Kim, "Short Channel MOS Transistor", University of Minnesota Dept. of ECE, USA
- [9] N. Hanchate; N. Ranganathan, "LECTOR: a technique for leakage reduction in CMOS circuits," IEEE Transactions on Very Large Scale Integration (VLSI) systems, Volume: 12, Issue: 2, Feb. 2004
- [10] Lin Yuan and Gang Qu, "A Combined Gate Replacement and Input Vector Control Approach for Leakage Current Reduction, IEEE Transactions on Very Large Scale Integration (VLSI) Systems", Volume: 14, Issue: 2, Feb. 2006
- [11] Jonathan P. Halter and Farid N. Najm, "A Gate-Level Leakage Power Reduction Method for Ultra-Low-Power CMOS Circuitst", Proceedings of CICC 97 -Custom Integrated Circuits Conference, May 1997
- [12] A.J.Prasad, 2ABbadasari, "Input Vector Control Approach for Leakage Reduction and Low Power Consumption", International journal of electronics and communication technology(IJECT)-Vol. II,SP-1, Dec 2011

- [13] Lei cheng, Liangdeng,"A Fast Simultaneous Input Vector Generation and Gate Replacement Algorithm for LeakagePower Reduction.",In DAC july 24-28 2006
- [14] V.LeelaRani, M.Madhavi Latha, "Implementation of genetic algorithm for Minimum leakage vector in input vector control approach", IEEE conference, SPACES, Jan 2015
- [15] V.Leela Rani and M.Madhavi Latha, "particle Swarm Optimization Algorithm for Leakage Power Reduction in VLSI Circuits", INTL journal of electronics and telecommunications, 2016, Vol. 62, PP. 179-186 Manuscript received July 4, 2015; revised June, 2016
- [16] Afshin Abdollahi, Farzan Fallah, "Leakage Current Reduction in CMOS VLSI Circuits by Input VectorControl", IEEE Transactions on Very Large Scale Integration (VLSI) Systems archive Volume 12 Issue 2, February 2004
- [17] Swarup Bhunia, Saibal Mukhopadhyay, "Low-Power Scan Design Using First-Level Supply Gating", IEEE Transactions on very Large scale integration (VLSI) systems, Vol. 13, No. 3, March 2005
- [18] Youngsoo Shin, Seungwhun Paik, Hyung-Ock Kim, "Semicustom Design of Zigzag Power-Gated Circuits in Standard Cell Elements", IEEE Trascations on CAD Design of integrated Circuits and Systems, Vol. 28, No 03, March 2009.
- [19] Akhila Abba, K Amarender, "Improved Power Gating Technique for Leakage Power Reduction", Research Inventy: International Journal Of Engineering And Science, Vol.4, Issue 10, October 2014
- [20] Ismo Hänninen, "Low Power System-On-Chip Design, Chapter13: Retention Register Design", TAMPERE University of Technology, Aug 2009
- [21] "Chapter 5 Super-Cutoff Power Gating TCAM Design with Leakage Current Reduction"
 - [online]. Available: https://ir.nctu.edu.tw/bitstream/11536/80561/9/164909.pdf [accessed: 25-12-2018]
- [22] Silvaco Nangate 45nm open cell library
 [online] Available:
 https://www.silvaco.com/products/nangate/Library_Creator_Platform/index.htm
 1 [accessed: 2-12-2018]