

REFERENCES:

1. Eric Coutes."Practical Inductor,"Internet: www.learnabout-electronics.org/ac_theory/inducto03.php,Sep.04,2013 [Jan.25,2015]
2. Tavarez, A. *et al*, "Modeling the thermal behavior of solder paste inside reflow ovens," *Journal of Electronic Packages*, vol.125 (2003), pp.335-346.
3. Maheney, H. V., "Thermal modelling of the infrared reflow process for solder ball connect (SBC)," *IBMJ Res. Develop.*, vol.37, no.05, (1993), pp.609-619.
4. S. Haddadi.(2007. Oct). "Processed Power Inductors shine at high frequencies," *Power Electronic Technology.[on-line]*. 38(1), pp.33-36 Available: www.powerelectronics.com [Dec.1,2013]
5. M. Gerber, J .A. Ferreira, I. W. Hofsajer, and N. Seliger, "A high-density heat-sink-mounted inductor for automotive application," *IEEE Trans. Ind.Appl.*, vol.40, no.4, pp.1031-1038, Jyl/Aug.2004.
6. R. Worbel, N. McNeill, and P. H. Mellor,. "Performance analysis and thermal modelling of a high-energy-density prebiased inductor," *IEEE Trans. Ind.Electron.*, vol.57, no.1, pp.201-208, Jan.2010.
7. W. G. Odendaal, J.Azevedo, G. W. Brunning, and R. M. Wolf, "A high-efficiency mangentic component with superior calorimetric performance for low-profile high density power conversion." *IEEE Trans. Ind.Appl.*, vol.40, no.5, pp. 1287-1293, Sep./Oct.2004.
8. S. Wang, M. A. de Rooji, W.G. Odendaal, J. D. van Wyk, and D. Boroyevich, "Reduction of high-frequency conduction losses using a planar Litz structure," *IEEE Trans. Power Electron.*, vol. 20, no. 02, pp. 261-267, Mar. 2005.
9. G. L. Skibinski, B. G. Schram, J. R. Brauer, and Z. Badics, "Finite element prediction of losses and temperatures of laminated and composite inductors for AC drives," in *Proc. IEEE IEMDC*, Jun. 1–4, 2003, pp. 756–763.
10. X. Mao, W. Chen, and Y. Li, "Winding loss mechanism analysis and design for new structure high-frequency gapped inductor," *IEEE Trans. Magn.*, vol. 41, no. 10, pp. 4036–4038, Oct. 2005.

11. J. Fletcher, B. Williams, and M. Mahmoud, "Airgap fringing flux reduction in inductors using open-circuit copper screens," *Proc. Inst. Elect. Eng.—Elect. Power Appl.*, vol. 152, no. 4, pp. 990–996, Jul. 2005.
12. K. Nakamura, H. Yoshida, and O. Ichinokura, "Electromagnetic and thermal coupled analysis of ferrite orthogonal-core based on threedimensional reluctance and thermal resistance network model," *IEEE Trans. Magn.*, vol. 40, no. 4, pp. 2050–2052, Jul. 2004.
13. G. R. Kamath, "An electrical circuit based 3-D thermal model of a fan cooled 600 μ H, 80 A inductor for a plasma cutting power supply," in *Proc. IEEE 23rd Annu. APEC*, Feb. 24–28, 2008, pp. 402–408.
14. R.Wrobel, and P.H. Mellor, "Thermal design of high-energy density wound components," *IEEE Trans. Ind.Electron.*, vol.58, no.9, pp.4096-4104, Sep.2011.
15. IPC/JEDEC. "Moisture/Reflow sensitivity classification for nonhermetic solid state surface mount devices," IPC/JEDEC J-STD-020D.1, March.1, 2008.
16. M. Inoue and T. Koyanagawa. "Thermal simulation for predicting substrate temperature during reflow soldering process," presented at Electronic Components and Technology Conference, Yokohoma, Japan, 2005.
17. Nakao. H, Hiraizumi. A, and Iwasaki, E., "Reflow oven for a Pb-free Soldering Process," *Furukawa Review*, No 20, pp. 77-82, 2001.
- 17 D.A.Staton and A.Cavagnino,"Convection heat transfer and flow calculations suitable for electric machines thermal models," *IEEE Trans. Ind.Electron.*, vol.55, no.10, pp.3509-3516, Oct.2008.
- 18 J.H.Lienhard, "Modes of heat transfer," in *A heat transfer text book*, 3rd ed, vol 1, J.H.Lienhard, Ed.Cambridge,2003, pp.10-35.
- 19 Zhuqing Zhang; Sitaraman, S.K.; Wong, C.P., "FEM modeling of temperature distribution of a flip-chip no-flow under fill package during solder reflow process," *Electronics Packaging Manufacturing, IEEE Transactions on* , vol.27, no.1, pp.86-93, Jan. 2004

- 20 Balazs Illes. Gabor Harsanyi, “3D mapping of forced convection efficiency in reflow ovens, “presented at the Periodic. Polytechnica. Elec. Eng., Vol. 52, No. 1-2, pp. 59-65, (2008).
- 21 K.L. Lawrence. “Heat transfer and thermal stresses,” in *ANSYS workbench tutorial*, 13 release, K.L. Lawrence, Ed.India:SDC publication,2011,pp.7.1-7.26.
- 22 Colonel Wm. T. McLyman. “DC inductor design using powder cores,” in *Transformer and inductor design hand book*, 3rd edition, Ed.USA:Library of congress cataloging-in-publication data, 2004, chapter 9.
- 23 J.Hu, C.R.Sullivan, “AC resistance of planar power inductors ad the quasidistributed gap techniques,” *IEEE Trans. Power.Electron.*, vol.16, no.04, pp.558-567, Jul.2004.