A GAP CALCULATION METHOD TO MINIMIZE INDUCTANCE DROP DURING REFLOW ON LOW COST HIGH CURRENT HELICAL WOUND PLANAR POWER INDUCTOR

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DECLARATION

I declare that this is my own work and this dissertation does not incorporate without acknowledgement any material previously submitted for a degree or diploma in any other university or institute of higher learning and to the best of my knowledge and believe it does not contain any material previously published or written by another person except where the acknowledgement is made in the text.

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Dr. D.P.Chandima

ABSTRACT

Power inductors are widely used in many power electronic applications such as voltage regulator modules, DC-DC converters and battery power systems. Recently electronic industry advancement shows an increasing trend in usage of low cost high current helical wound planar power inductors also known as processed power inductors. The new trend and competition in electronic industry is initiating to design and manufacture power inductors in high volume in a short processing time. The quasi-planar winding technique gives compact size and rectangular cross section is giving low heat dissipation while reducing AC/DC resistance. The above significance and requirement tend to design custom made different rating inductors. There is a problem in these types of inductors, a inductance drop after reflow soldering process as mostly these inductors are surface mount device. This is happening due to inadequate gap between helical wound coil conductor and upper core inner surface. The inadequate gaps are not only causing inductance drop, beyond that core separation as well. Therefore formulating an iterative equation to calculate gap to minimize and control inductance drop during reflow and operation for different rated power inductors during design and manufacturing stages will give a prominent solutions for processed inductor designers and manufacturers. The methodology is mathematically model the reflow and operational thermal model and calculate thermal directional strain that to be analyzed with ANSYS thermal simulation. Geometrically different five inductor models are selected. The inductance readings are recorded at both pre and post reflow simulation to calculate variation. The influencing parameters are identified with respect to core geometry, copper volume and dimension, direct exposing area of material to the thermal load during reflow and operations conditions considered as well. The samples have arranged with respect to inductance drop in an increasing manner and identified parameters have plotted along with inductance drop to find trends lines. The trend line relationships are combined together to formulate equation with a constant. The equations have validated with samples.

DEDICATION

To my wife and Etal Group (PVT) Ltd

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LIST OF ABBREVIATIONS

AC	-Alternating Current
DC	-Direct Current
VHF	-Very High Frequency
FM	-Frequency Modulation
JEDEC	-Joint Electronic Device Engineering Council
SMD	-Surface Mount Devices
FEM	-Finite Element Method
IR	-Infrared
SMT	-Surface Mount Technology
CAD	-Computer Aided Design
PCB	-Printed Circuit Board
3D	-Three dimensional
SST	-Steady State Thermal
L drop	-Inductance drop
NPI	-New Product Introduction